1. LINEAR WAVE SHAPING

Aim:

i) To design a low pass RC circuit for the given cutoff frequency and obtain its frequency response.

ii) To observe the response of the designed low pass RC circuit for the given square waveform for T<<RC,T=RC and T>>RC.

iii) To design a high pass RC circuit for the given cutoff frequency and obtain its frequency response.

iv) To observe the response of the designed high pass RC circuit for the given square waveform for T<<RC,T=RC and T>>RC.

Apparatus Required:

Name of the Component/Equipment	Specifications	Quantity
Resistors	1KΩ	1
	2.2KΩ,16 KΩ	1
Capacitors	0.01μF	1
CRO	20MHz	1
Function generator	1MHz	1

Circuit Diagram:

Low Pass RC Circuit :

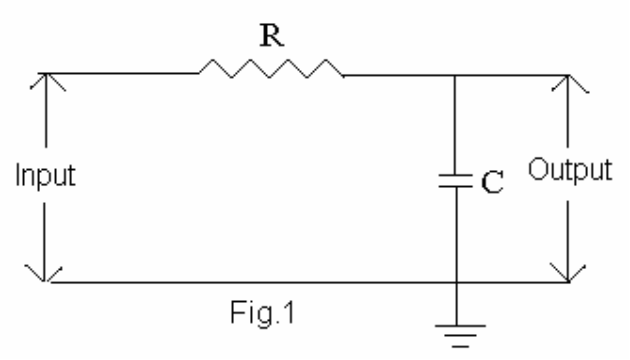


Fig.1

High Pass RC Circuit :

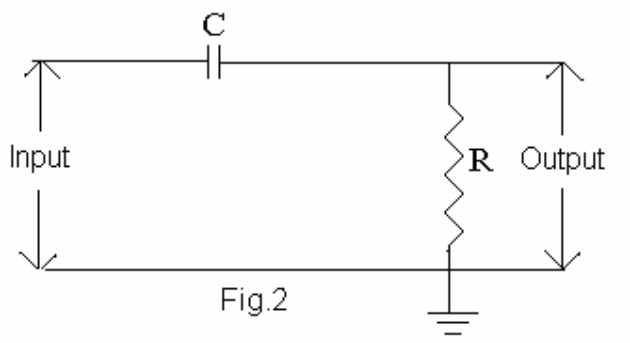


Fig.2

Procedure:

A) Frequency response characteristics:

1 .Connect the circuit as shown in Fig.1 and apply a sinusoidal signal of amplitude of 2V p-p as input.

2. Vary the frequency of input signal in suitable steps 100 Hz to 1 MHz and note down the p-p amplitude of output signal.

3. Obtain frequency response characteristics of the circuit by finding gain at each frequency and plotting gain in dB vs frequency .

4.Find the cutoff frequency f_c by noting the value of f at 3 dB down from the maximum gain

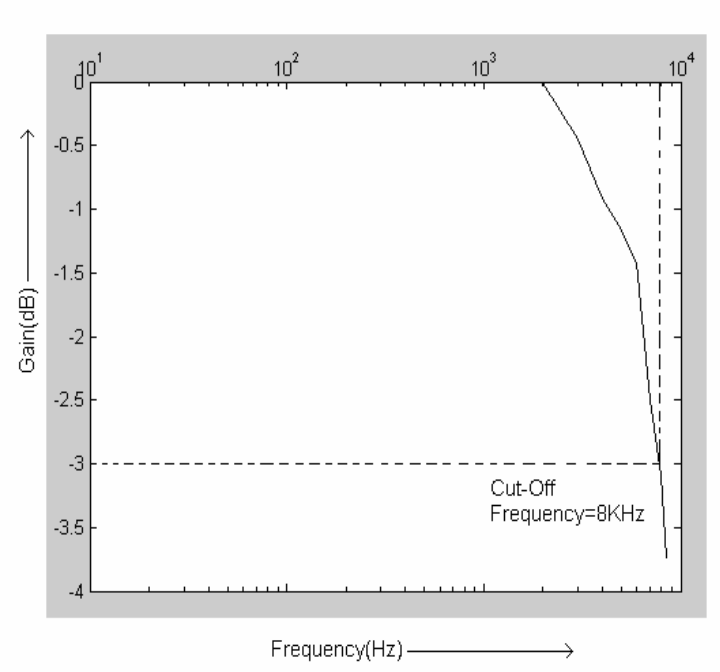
B)Response of the circuit for different time constants:

Time constant of the circuit RC= 0.0198 ms

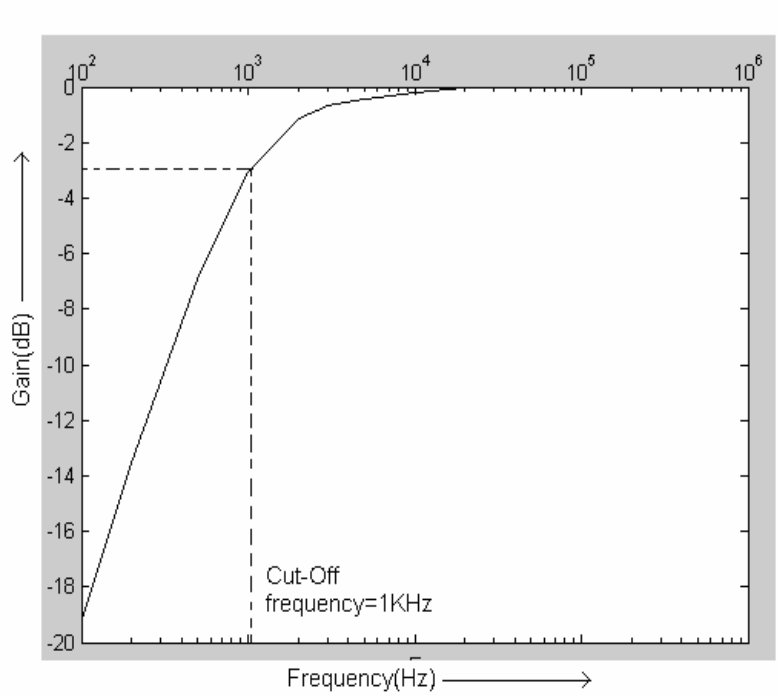
1. Apply a square wave of 2v p-p amplitude as input.
2. Adjust the time period of the waveform so that T>>RC, T=RC,T<<RC and observe the output in each case.
3. Draw the input and output wave forms for different cases.

Model Graphs and Wave forms

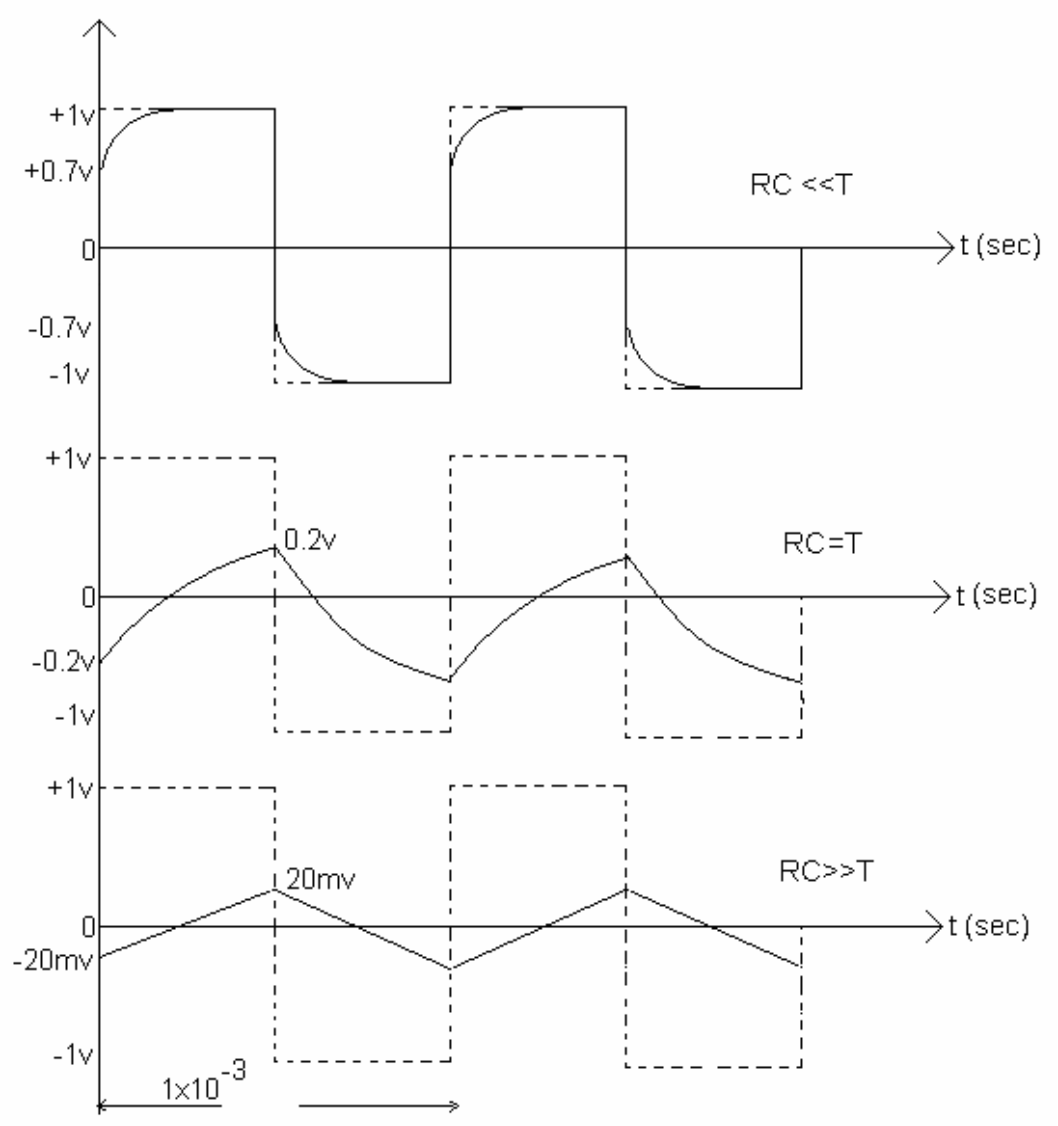
Low Pass RC circuit frequency response:



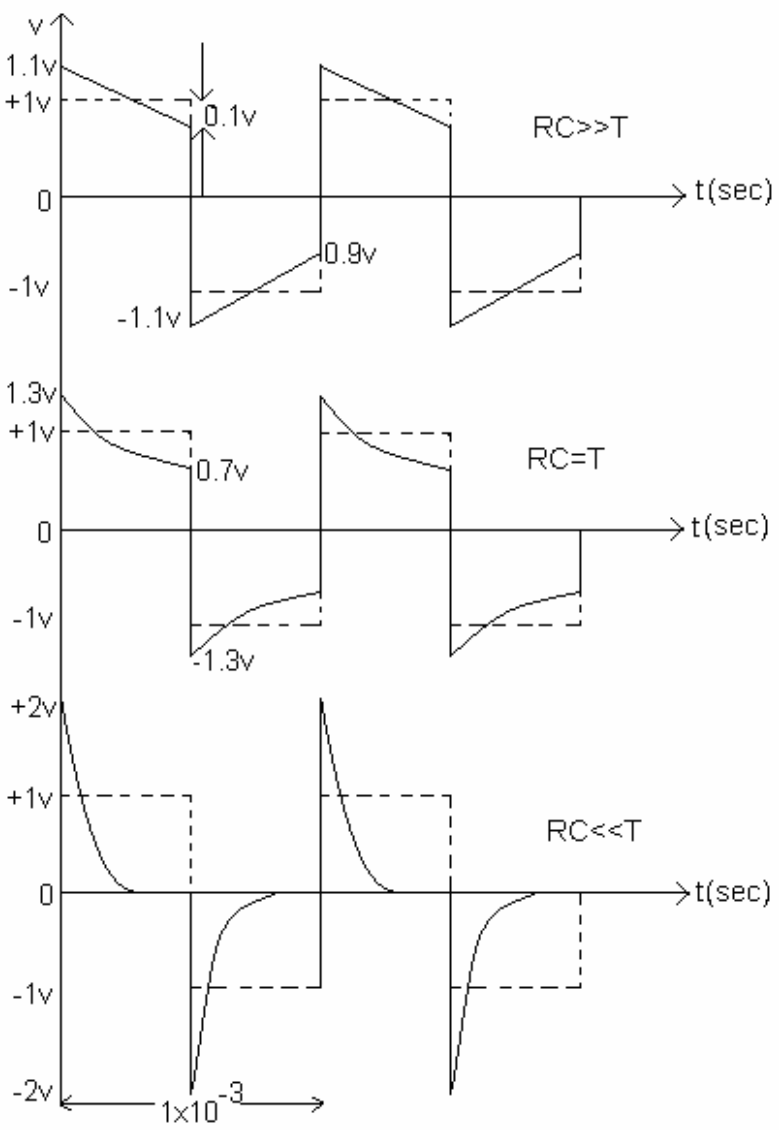
High Pass RC circuit frequency response:



Low Pass RC circuit



High Pass RC Circuit



2. NON LINEAR WAVE SHAPPING-CLIPPERS

Aim: To obtain the output and transfer characteristics of various diode clipper circuits.

Apparatus required:

Name of the Component/Equipment	Specifications	Quantity
Resistors	1KΩ	1
Diode	1N4007	1
CRO	20MHz	1
Function generator	1MHz	1
DC Regulated power supply	0-30V,1A	1

Circuit diagrams:

Positive peak clipper with reference voltage, V=2V

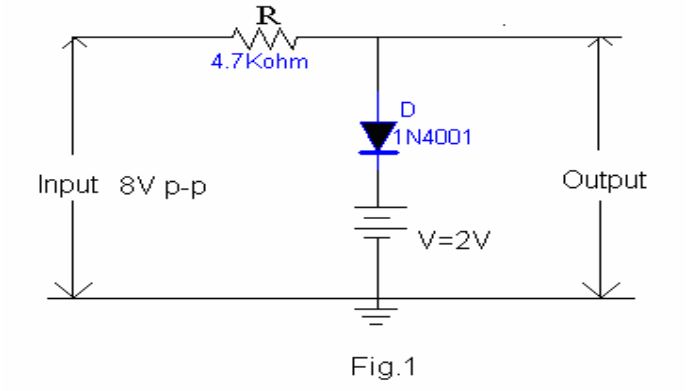


Fig.1

Positive Base Clipper with Reference Voltage, V=2V

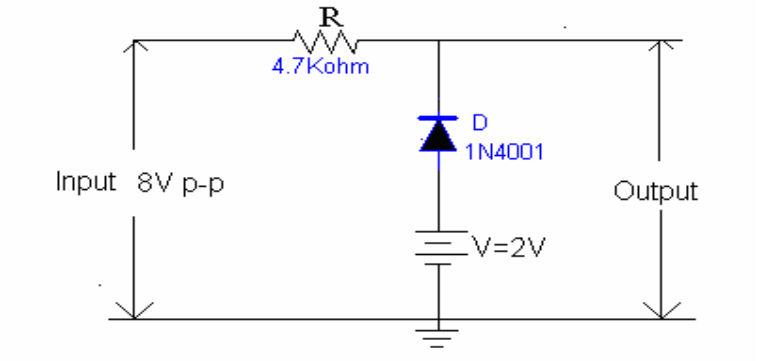


Fig.2

Negative Base Clipper with Reference Voltage,V=-2V

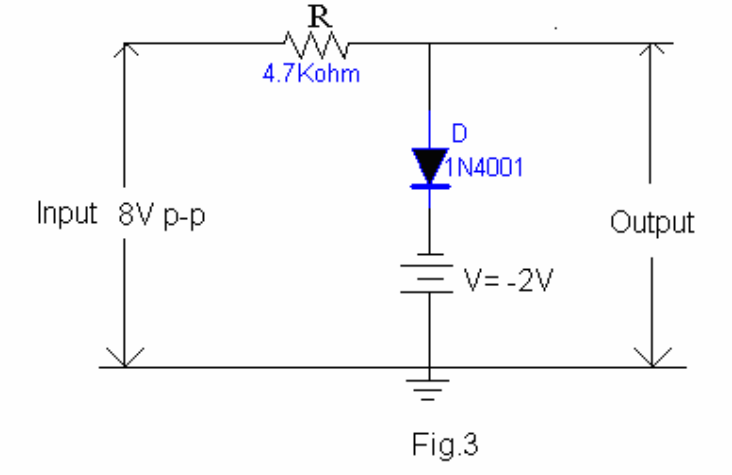


Fig.3

Negative peak clipper with reference voltage, V=-2v

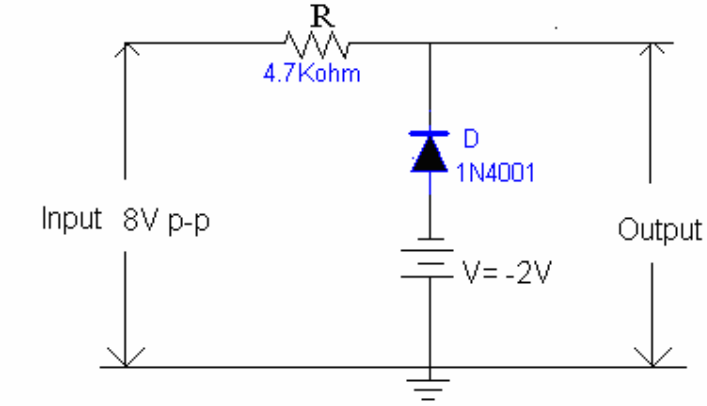


Fig.4

Slicer Circuit:

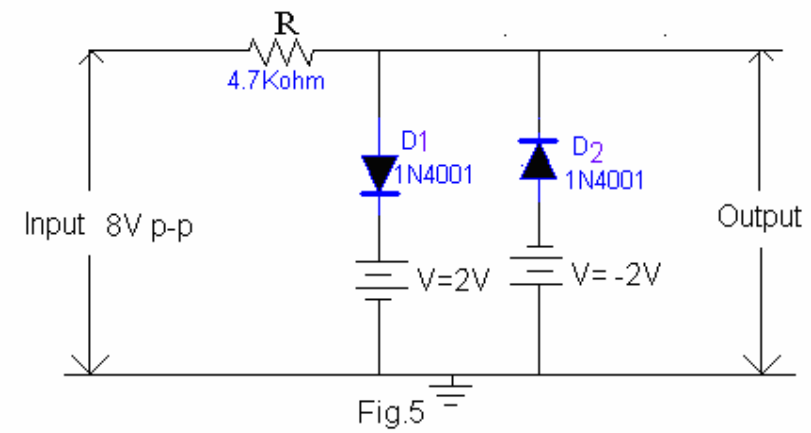


Fig.5

Procedure:

1.Connect the circuit as per circuit diagram shown in Fig.1

Obtain a sine wave of constant amplitude 8 V p-p from function generator and apply as input to the circuit.

2.Observe the output waveform and note down the amplitude at which clipping occurs.

3.Draw the observed output waveforms.

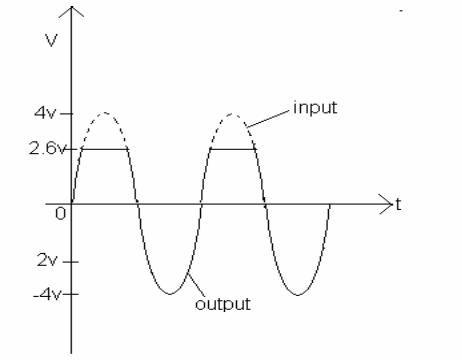
4. To obtain the transfer characteristics apply dc voltage at input terminals and vary the voltage insteps of 1V up to the voltage level more than the reference voltage and note down the corresponding voltages at the output.

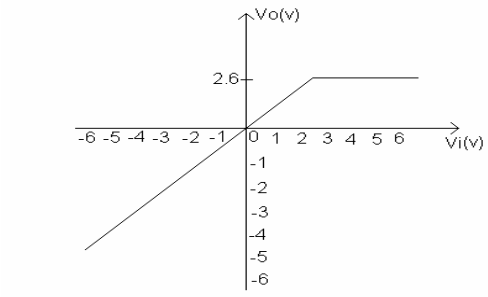
5. Plot the transfer characteristics between output and input voltages.

6. Repeat the steps 1 to 5 for all other circuits.

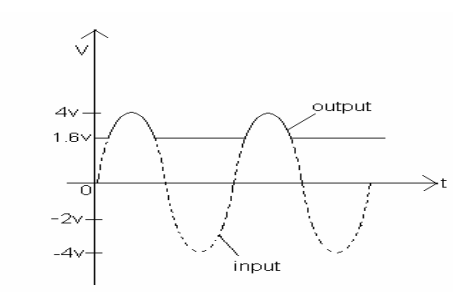
Model wave forms and Transfer characteristics

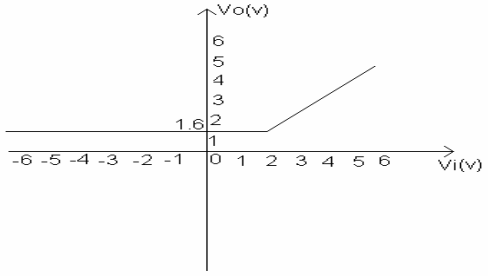
Positive peak clipper: Reference voltage V=2v



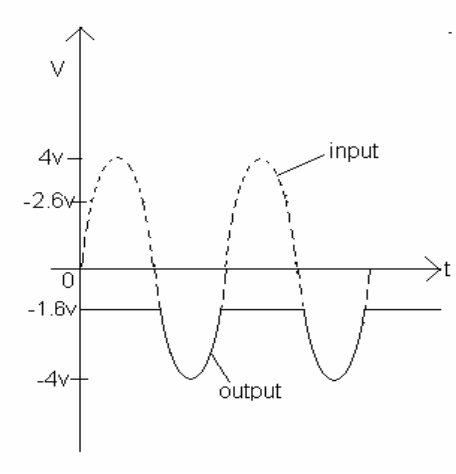


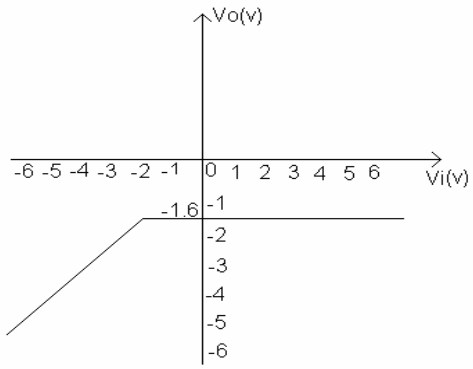
Positive base clipper: Reference voltage V=2v



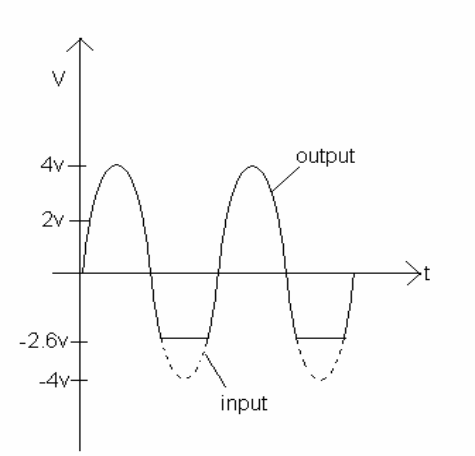


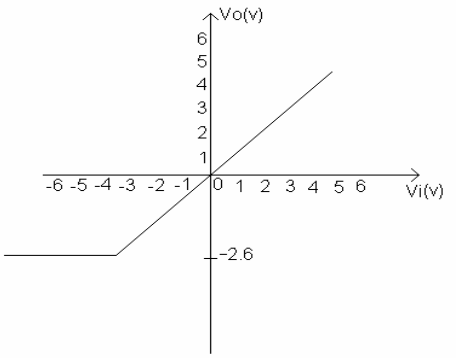
Negative base clipper: Reference voltage V=2v



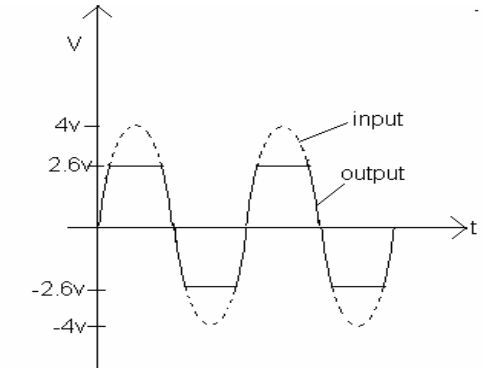


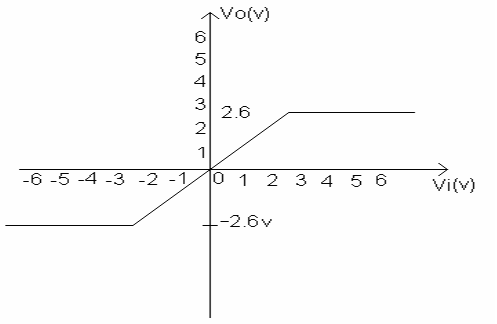
Negative peak clipper: Reference voltage V=2v





Slicer Circuit:





3.NON LINEAR WAVE SHAPPING-CLAMPERS

Aim: To verify the output of different diode clamping circuits.

Apparatus Required:

Name of the Component/Equipment	Specifications	Quantity
Resistors	10KΩ	1
Capacitor	100uF, 100pF	1
Diode	1N4007	1
CRO	20MHz	1
Function generator	1MHz	1

Circuit Diagrams

Positive peak clamping to 0V :

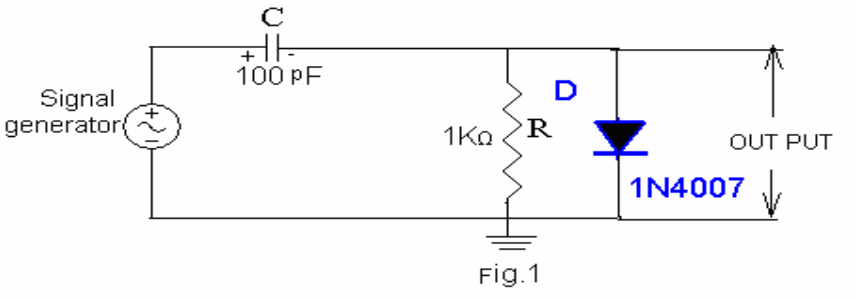


Fig.1

Positive peak clamping to V_r=2v

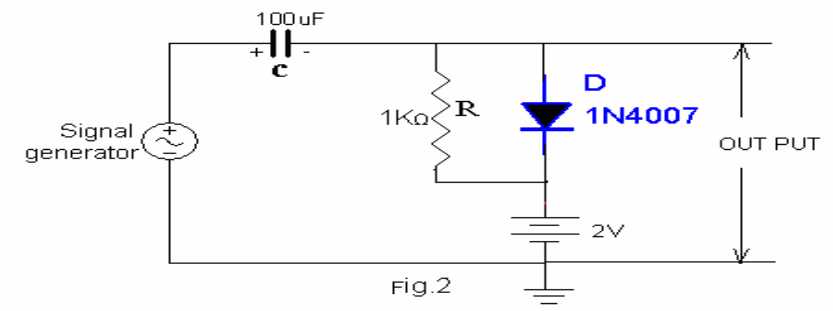


Fig.2

Negative peak clamping to V_r=0v

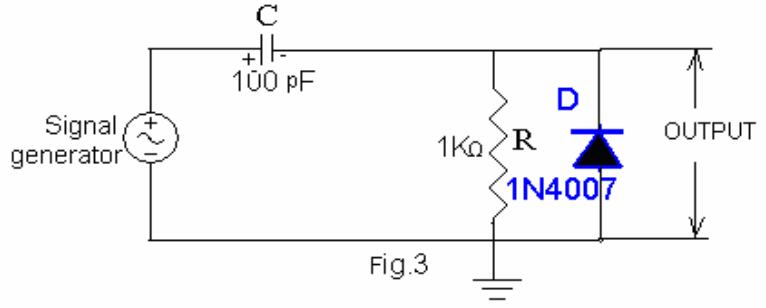


Fig.3

Negative peak clamping to V_r= -2v

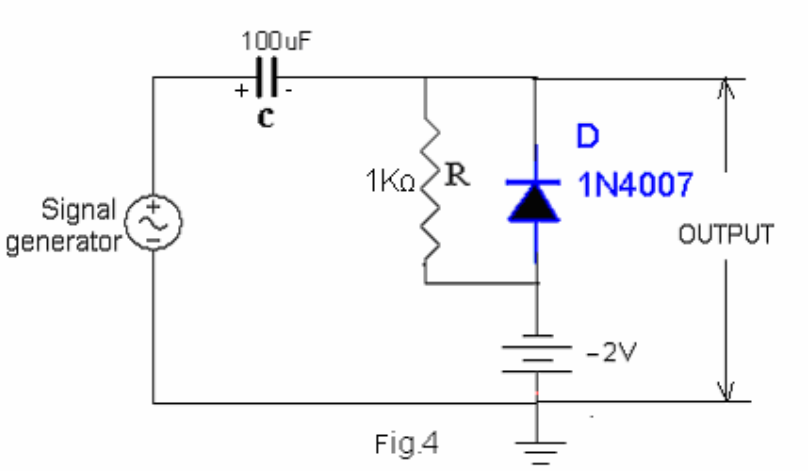


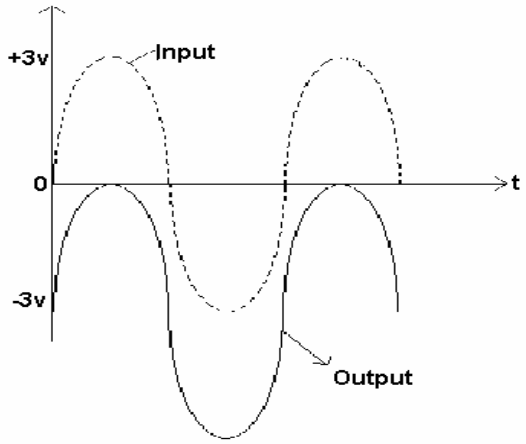
Fig.4

Procedure:

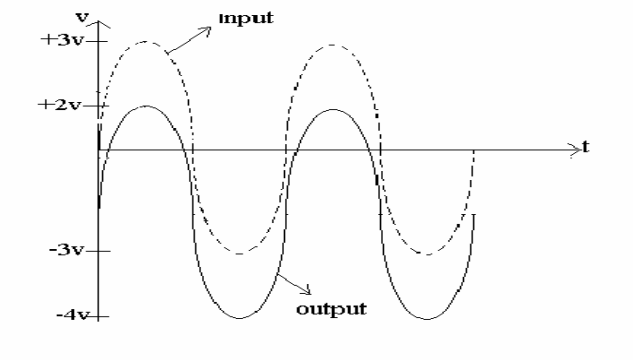
1. Connect the circuit as per circuit diagram.
2. Obtain a constant amplitude sine wave from function generator of 6 Vp-p, frequency of 1KHz and give the signal as input to the circuit.
3. Observe and draw the output waveform and note down the amplitude at which clamping occurs.
4. Repeat the steps 1 to 3 for all circuits.

Model waveforms:

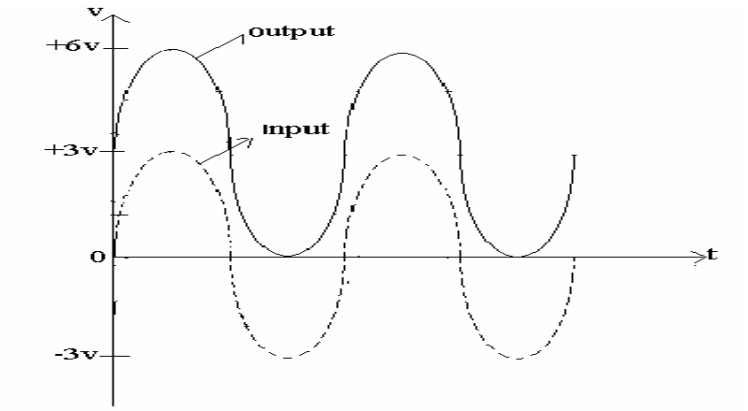
Positive peak clamping to 0V:



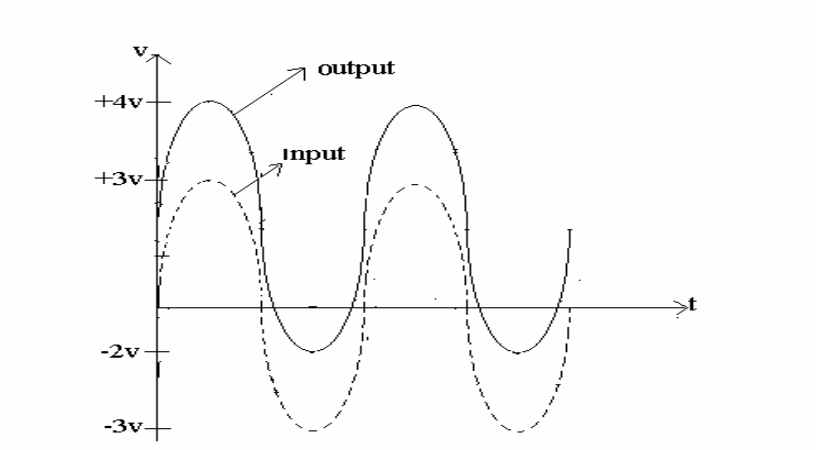
Positive peak clamping to V_r=2V



Negative peak clamping to 0V



Negative peak clamping to Vr= -2V



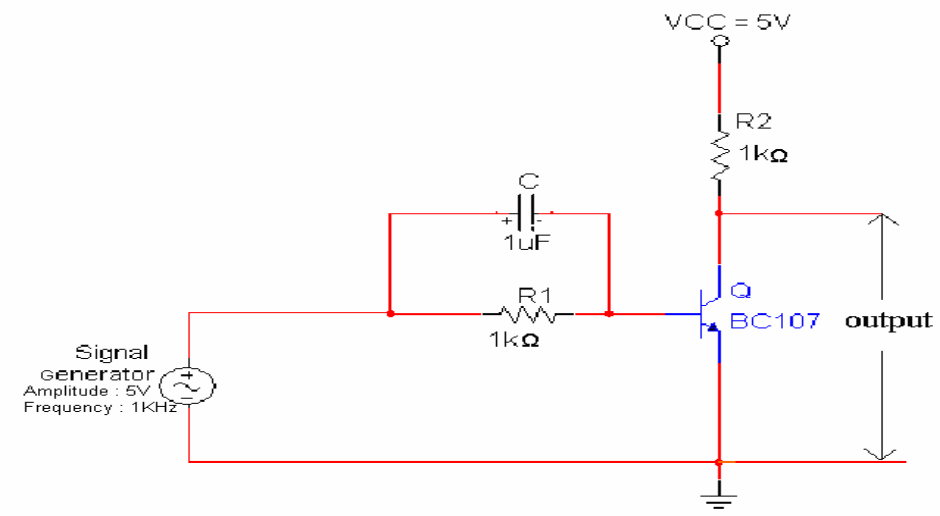
4. TRANSISTOR AS A SWITCH

Aim: To obtain characteristics of a transistor as a switch.

Apparatus Required:

Name of the Component/Equipment	Specifications	Quantity
Transistor	BC 107	1
Diode	0A79	1
Resistors	10K	2
	5.6KΩ	2
Capacitor	100pF	1
CRO	20MHz(BW)	1
Function generator	1MHz	1
Regulated Power Supply	0-30V, 1A	1

Circuit Diagram:



Procedure:

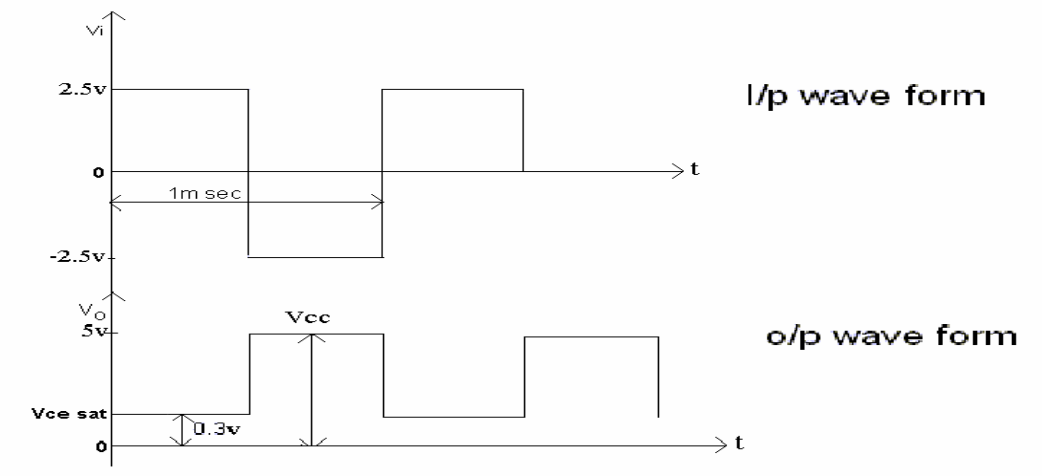
1.Connect the circuit as per circuit diagram.

2.Obtain a constant amplitude square wave from function generator of 5V p-p and give the signal as input to the circuit.

3.Observe the output waveform and note down its voltage amplitude levels.

4.Draw the input and output waveforms

Model graph:


Vi
2.5v
0
t
1m sec
-2.5v
I/p wave form
Vo
5v
Vcc
Vce sat
0.3v
0
t
o/p wave form

5. STUDY OF LOGIC GATES

Aim: To construct the basic and universal gates using discrete components and verify truth table.

Apparatus required:

Name of the Component/Equipment	Specifications	Quantity
Transistor	BC 107	1
Diode	IN4007	1
Resistors	4.7KΩ	2
	100KΩ	1
LED	-	1
Bread Board	-	1
Regulated Power Supply	0-30V, 1A	1

Circuit diagrams:

1. OR GATE

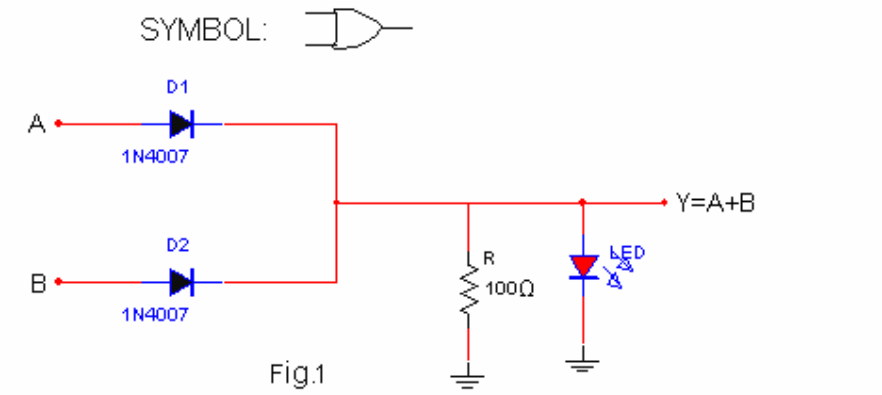


Fig.1

2.AND GATE

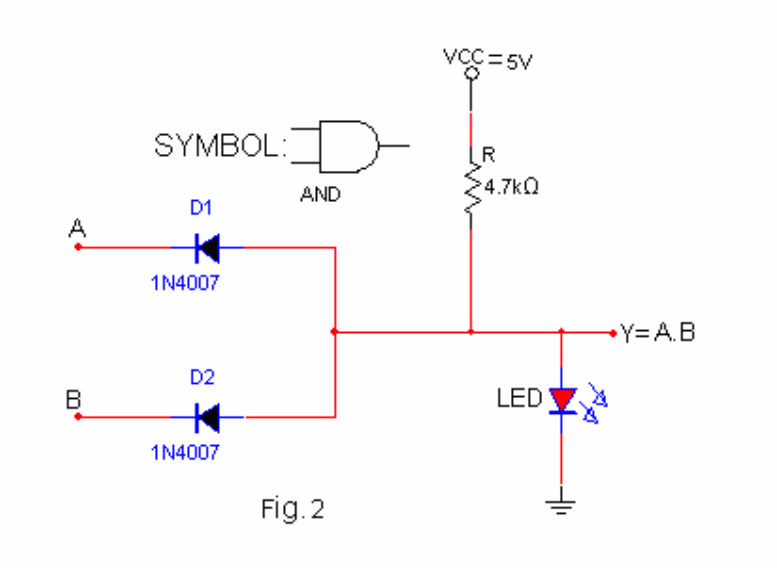


Fig. 2

3. NOT GATE:

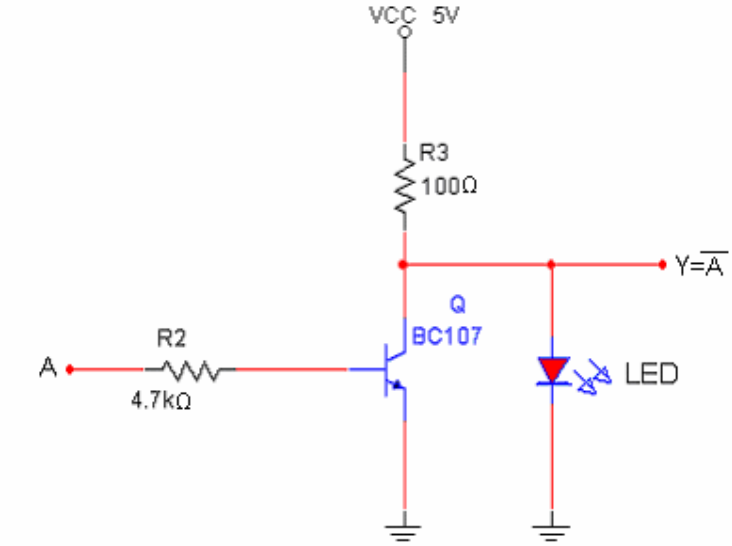


Fig.3

4. NOR GATE:

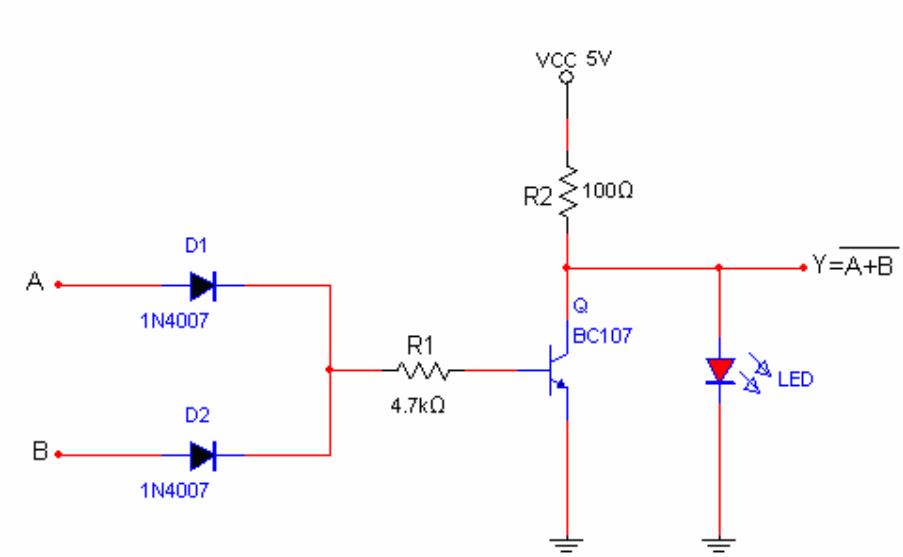


Fig.4

5. NAND GATE:

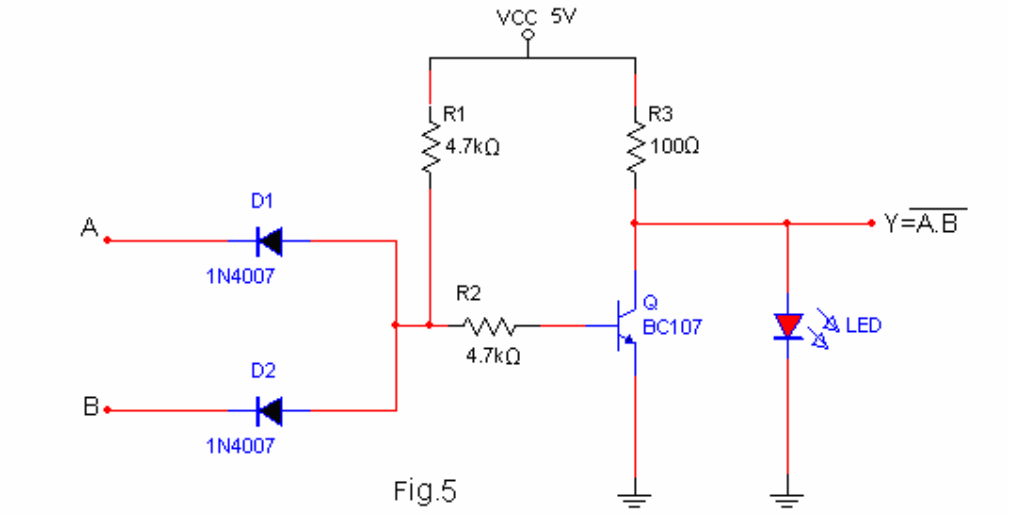


Fig.5

Truth tables:

1.AND GATE:

A	B	Y=AB
0	0	0
1	0	0
0	1	0
1	1	1

2. OR GATE:

A	B	Y=A+B
0	0	0
1	0	1
0	1	1
1	1	1

3. NOT GATE:

A	Y=~A
0	1
1	0

4. NAND GATE

A	B	Y=~(AB)
0	0	1
1	0	1
0	1	1
1	1	0

5. NOR GATE

A	B	Y=~(A+B)
0	0	1
1	0	0
0	1	0
1	1	0

6. STUDY OF FLIP FLOPS

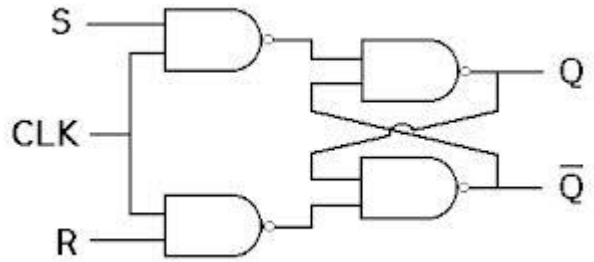
Aim: To verify truth tables of D and T flip-flops.

Apparatus required:

Name of the Component/Equipment	Specifications	Quantity
IC 7476	-	1
IC 7404	-	1
Digital Trainer	-	1

Circuit diagrams:

D-Flip Flop:

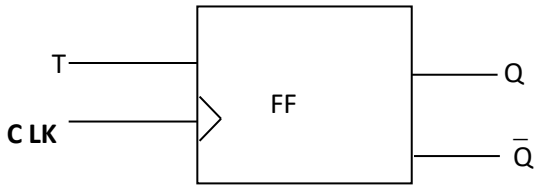


D- Flip Flop Truth Table:

Input	Previous state		Present state	
D	Q_1		Q_1	
0	0	1	0	1
1	1	0	1	0

T -Flip Flop:

SYMBOL FOR T-FLIP FLOP: -



T-FLIP FLOP USING JK FLIP FLOP:

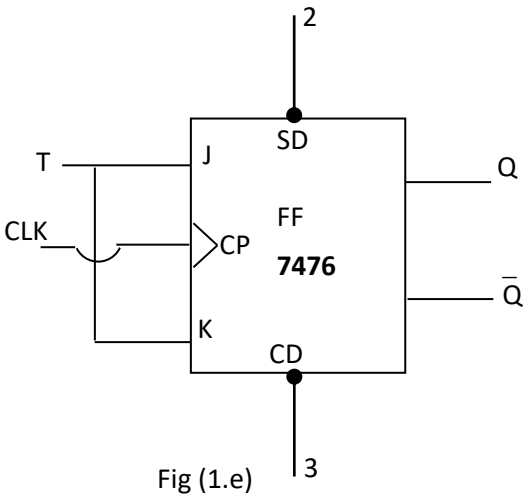
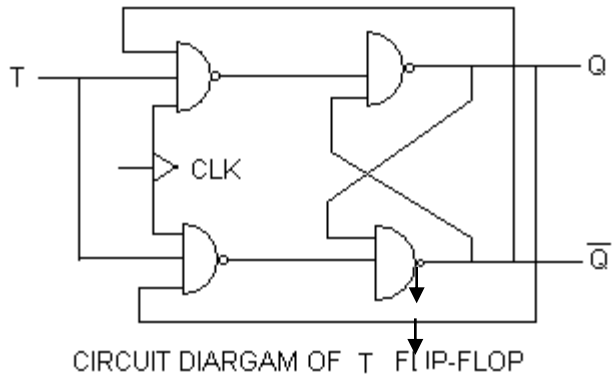


Fig (1.e)

TRUTH TABLE FOR T-FLIP FLOP: -



CIRCUIT DIARGAM OF T FLIP-FLOP

OUTPUTS	
Q	**$\bar{Q}$**
H	L
L	H
H	H
TOGGLE	
H	L
TOGGLE	

JK FLIP FLOP:

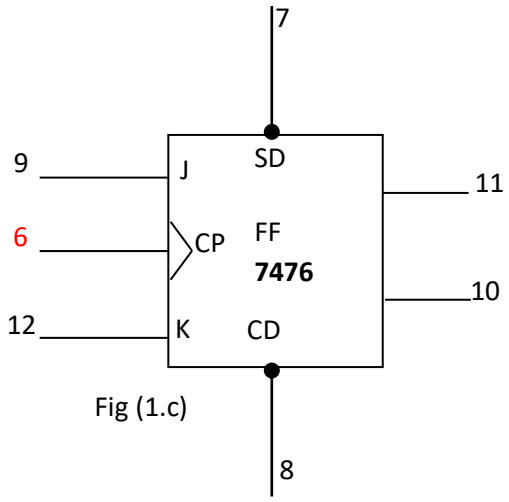


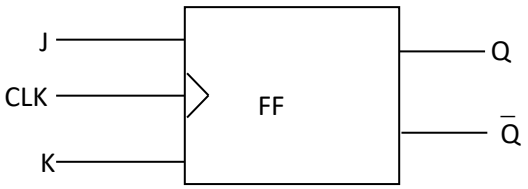
Fig (1.c)

TRUTH TABLE FOR JK-FLIP FLOP (IC 7476); -

SD Preset	CD Clear	Clock	J	K	OUTPUTS	
					Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$

*Unstable condition. It will not remain after C_n and P_n inputs return to their inactive (high) state

SYMBOL FOR JK FLIP FLOP:



Procedure:

D-Flip Flop

1. Place the required IC's on the bread board.

2. Connect V_{cc} (Power Supply) and Ground to the corresponding pin numbers of IC as shown in Appendix.

3. Connect the NOT gate 1& 2 terminals to 4 & 16 terminals of 7476 IC.

4. Apply input voltages 0 volts for logic 0 , 5 volts for logic 1.

5. Verify the truth table of D Flip Flop .

T-Flip Flop

1. Place the required IC's on the bread board.
2. Connect V_{cc} (Power Supply) and Ground to the corresponding pin numbers of IC as shown in Appendix.
3. Short the 4 & 16 terminals of 7476 IC.
4. Apply input voltages 0 volts for logic 0 , 5 volts for logic 1.
5. Verify the truth table of T Flip Flop

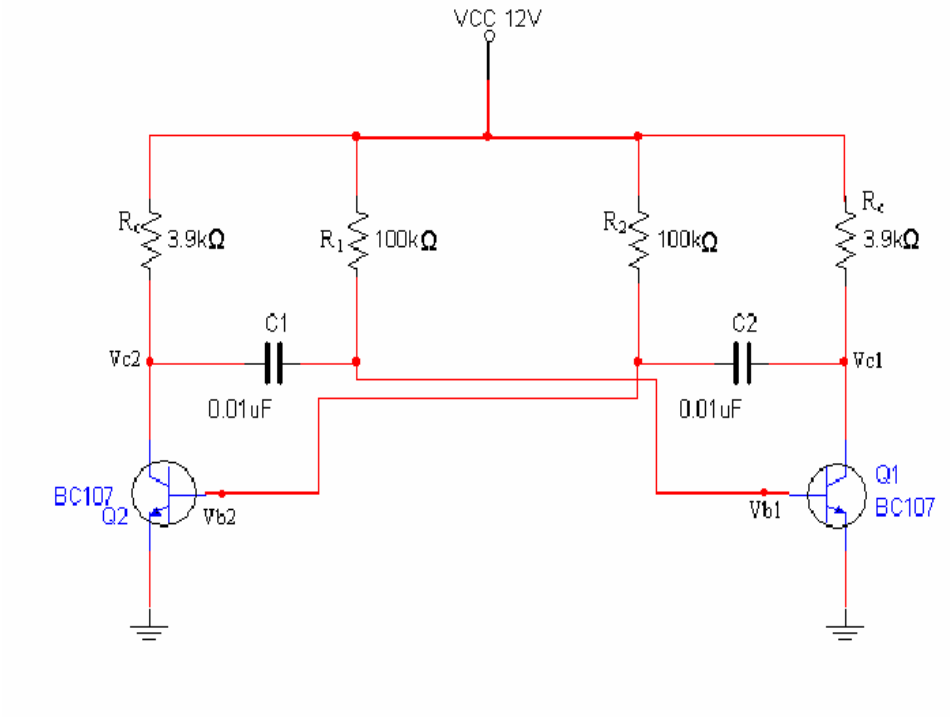
7. ASTABLE MULTIVIBRATOR

Aim: To Observe the ON & OFF states of Transistor in an Astable Multivibrator.

Apparatus required:

Name of the Component/Equipment	Specifications	Quantity
Transistor (BC 107)	BC 107	2
Resistors	3.9KΩ	2
	100KΩ	2
Capacitor	0.01µF	2
Regulated Power Supply	0-30V, 1A	1

Circuit Diagram



Procedure :

1. Calculate the theoratical frequency of oscillations of the circuit.

2.Connect the circuit as per the circuit diagram.

3 Observe the voltage wave forms at both collectors of two transistors simultaneously.

4. Observe the voltage wave forms at each base simultaneously with corresponding collector voltage.

5. Note down the values of wave forms carefully.

6. Compare the theoratical and practical values.

Calculations:

Theoritical Values :

$RC = R_1C_1 + R_2C_2$

Time Period, $T = 1.368RC =$

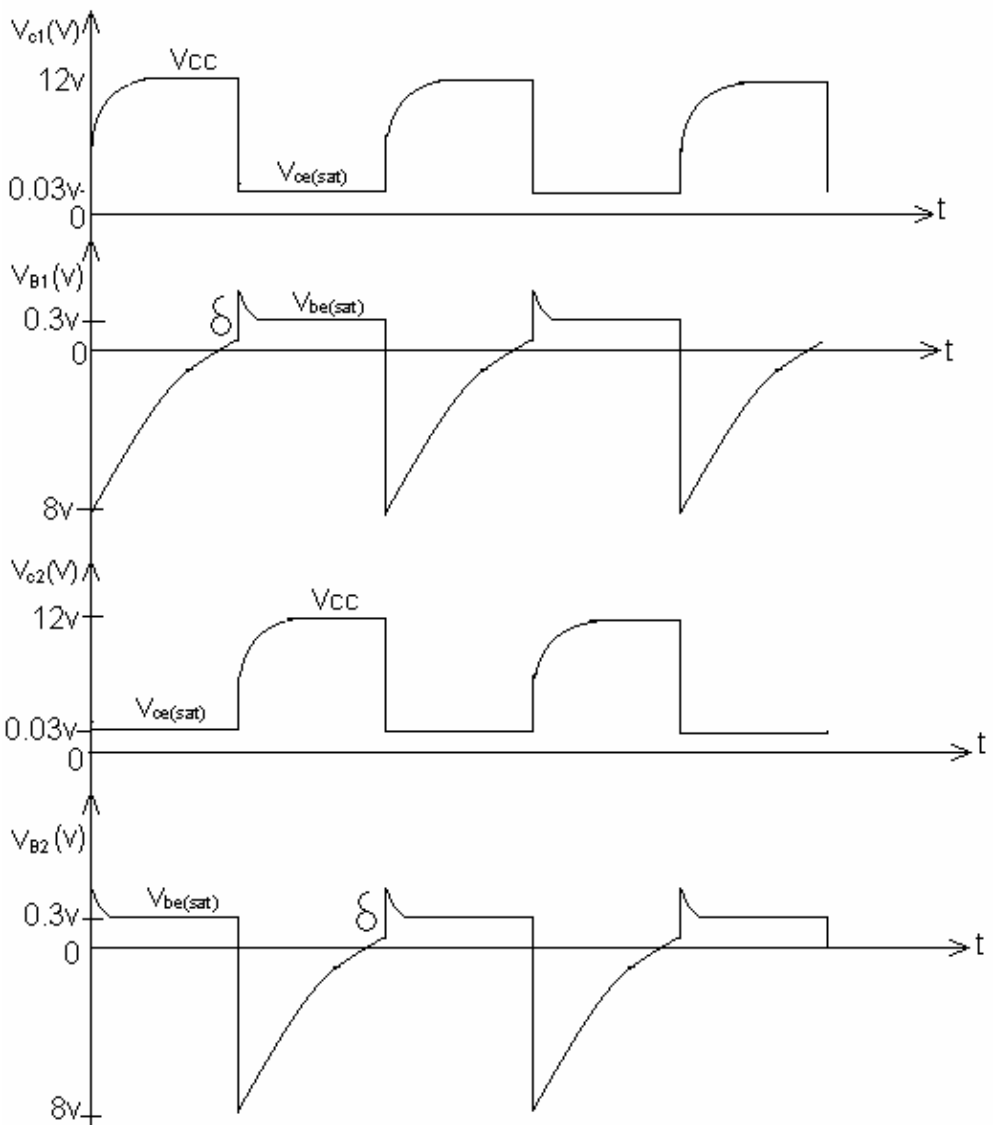
$1.368 \times 100 \times 10^{3} \times 0.01 \times 10^{-6} = 93$

μ sec

= 0.093 m sec

Frequency, $f = 1/T = 10.75kHz$

Model waveforms :



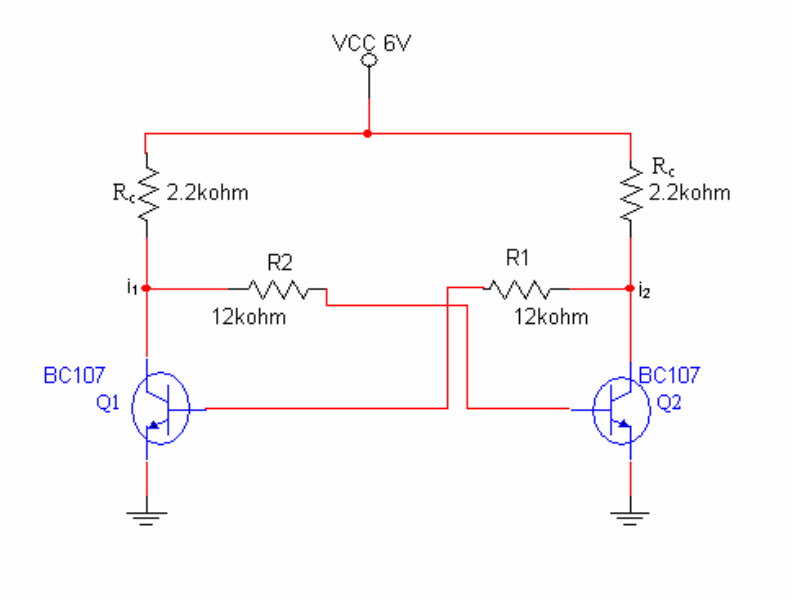
8. BISTABLE MULTIVIBRATOR

Aim: To Observe the stable states voltages of Bi stable Multi vibrator.

Apparatus required:

Name of the Component/Equipment	Specifications	Quantity
Transistor	BC 107	2
Resistors	2.2KΩ	2
	12KΩ	2
Regulated Power Supply	0-30V, 1A	1

.Circuit Diagram:



Procedure:

1. Connect the circuit as shown in figure.
2. Verify the stable state by measuring the voltages at two collectors by using multimeter.
3. Note down the corresponding base voltages of the same state (say state-1).
4. To change the state, apply negative voltage (say-2v) to the base of on transistor or positive voltage to the base of transistor (through proper current limiting resistance).
5. Verify the state by measuring voltages at collector and also note down voltages at each base.

Observations :

Sample Readings

Before Triggering

Q_1(OFF)	Q_1(ON)
V_{BE1}=0.03V	V_{BE2}=0.65V
V_{CE1}=5.6V	V_{CE2}=0.03V

After Triggering

Q_1(ON)	Q_1(OFF)
V_{BE1}=0.65V	V_{BE2}=0.01V
V_{CE1}=0.03V	V_{CE2}=5.6V

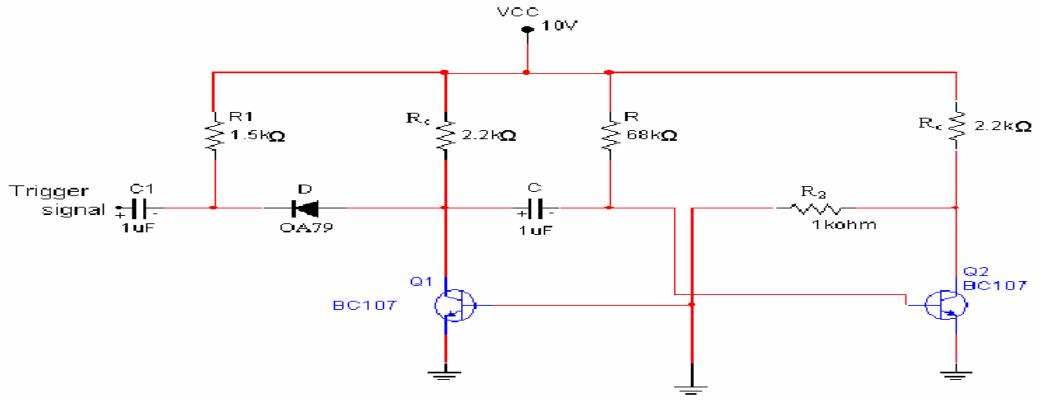
9. MONOSTABLE MULTIVIBRATOR

Aim: To observe the stable state and quasi stable state voltages in mono stable Multi vibrator.

Apparatus Required:

Name of the Component/Equipment	Specifications	Quantity
Transistor (BC 107)		2
Resistors	1.5KΩ	1
	2.2KΩ	2
	68KΩ	1
	1KΩ	1
Capacitor	1µF	2
Diode	0A79	1
CRO	20MHz	1
Function generator	1MHz	1
Regulated Power Supply	0-30V, 1A	1

.Circuit Diagram:



Procedure:

1. Connect the circuit as per the circuit diagram.

2. Verify the stable states of Q_1 and Q_2

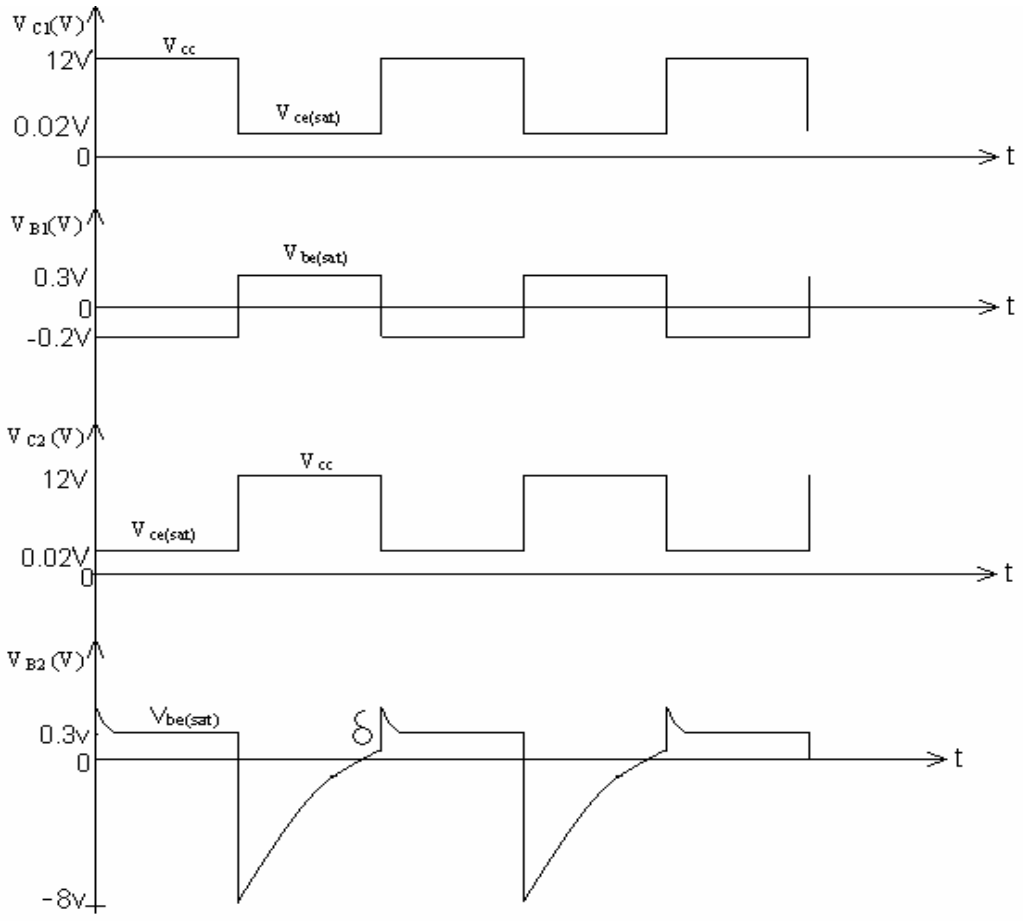
3. Apply the square wave of 2v p-p , 1KHz signal to the trigger circuit. 4

Observe the wave forms at base of each transistor simultaneously.

5. Observe the wave forms at collectors of each transistors simultaneously. 6.. Note down the parameters carefully.

7 Note down the time period and compare it with theoretical values. 8. Plot wave forms of V_{b1}, V_{b2},V_{c1} & V_{c2} with respect to time .

Model waveforms:



Calculations:

Theoretical Values:

Time Period, $T = 0.693RC$

$= 0.693 \times 68 \times 10^{3} \times 0.01 \times 10^{-6} =$

47μ sec

$= 0.047$ m sec

Frequency, $f = 1/T = 21$ kHz

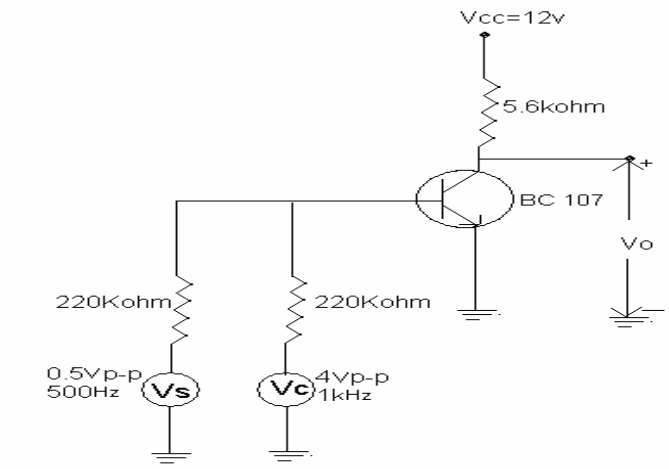
10. SAMPLING GATES

Aim: To observe the output of a bidirectional sampling gate for given input of a sine wave with a gating signal of square wave.

Apparatus Required:

Name of the Component/Equipment	Specifications	Quantity
Transistor (BC 107)	-	1
Resistors	220KΩ	1
	5.6Ω	1
CRO	20MHz	1
Function generator	1MHz	2
Regulated Power Supply	0-30V, 1A	1

Circuit diagram:



Procedure:

1. Connect the circuit as per the diagram.

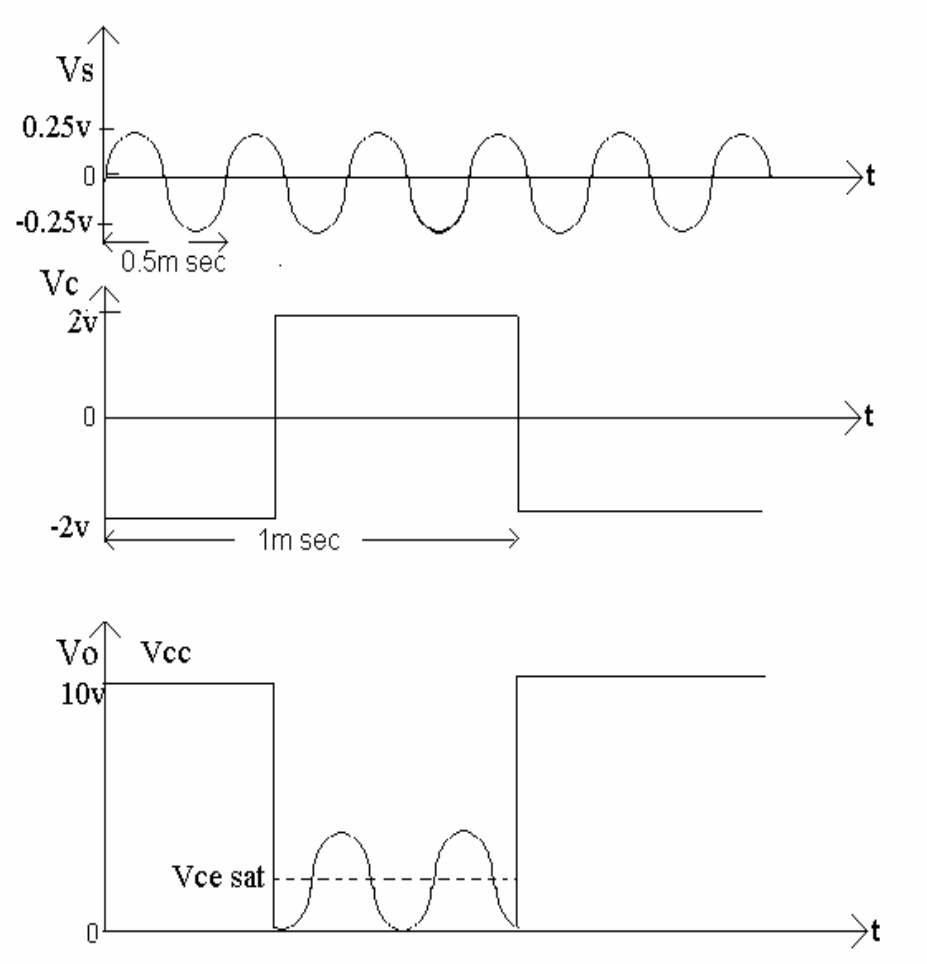
2. Generate a control voltage Vc of 4V peak to peak voltage 1KHz and apply it to the circuit.

3. Apply the input signal with a small peak to peak voltage.

4 Observe the output wave forms and Vc simultaneously and note down the parameters of waveforms.

5.Plot the graph between $V_{s,}V_c$ and output waveform with respect to time

Model wave forms:



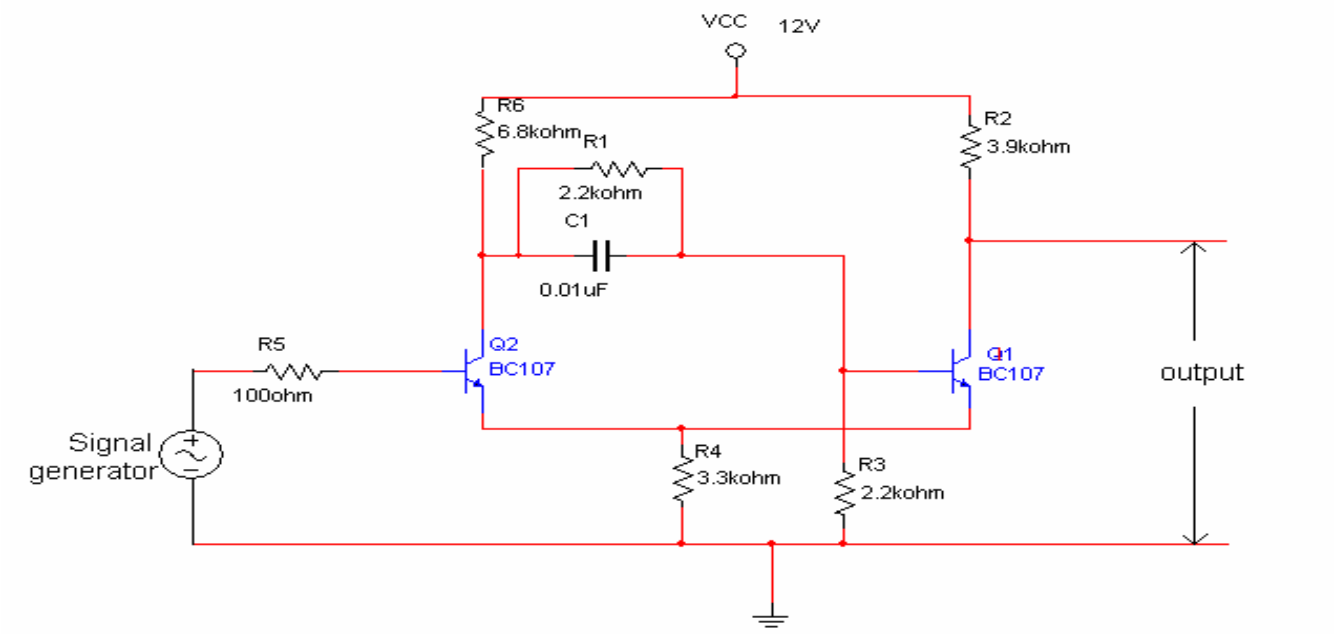
11.SCHMITT TRIGGER

Aim: To Generate a square wave from a given sine wave using Schmitt Trigger

Apparatus Required:

Name of the Component/Equipment	Values/Specifications	Quantity
Transistor	BC 107	2
Resistors	100Ω	1
	6.8KΩ	1
	3.9KΩ	1
	2.7KΩ	1
	2.2KΩ	1
Capacitor	0.01µF	1
CRO	20MHz	1
Regulated Power Supply	30V	1
Function generator	1MHz	1

Circuit diagram :



Procedure:

1 Connect the circuit as per circuit diagram.

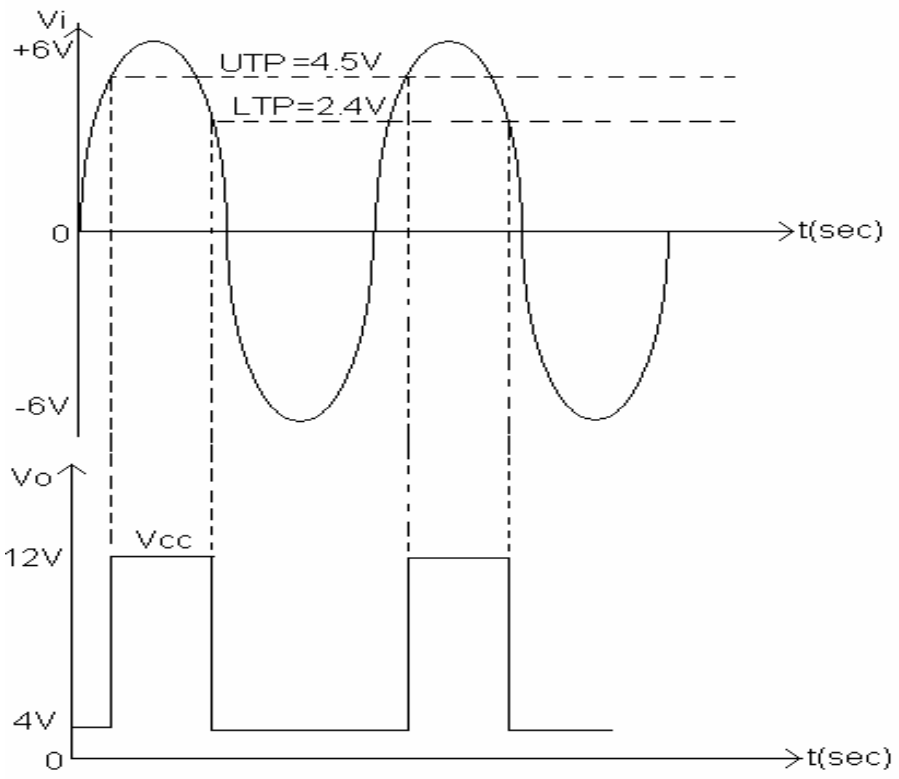
2 Apply a sine wave of peak to peak amplitude 10V, 1 KHz frequency wave as input to the circuit.

3 Observe input and output waveforms simultaneously in channel 1 and channel 2 of CRO.

4 Note down the input voltage levels at which output changes the voltage level.

5 Draw the graph between votage versus time of input and output signals.

Model Graph:



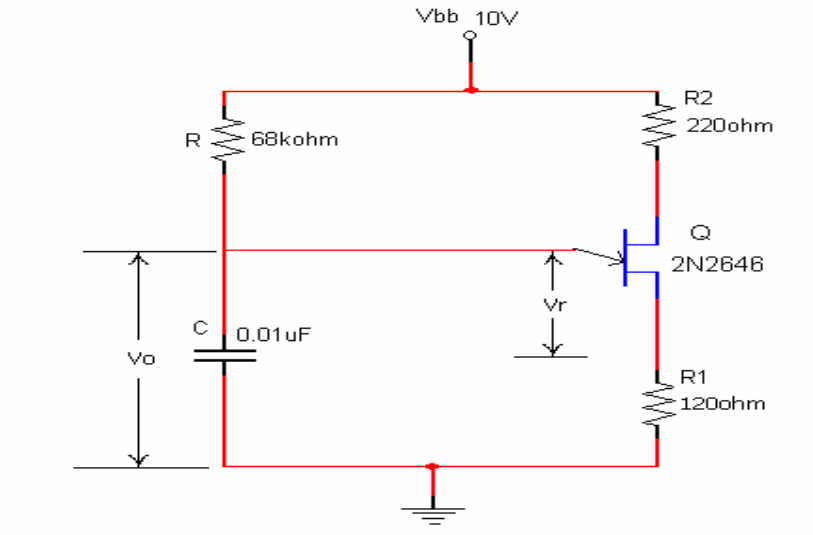
12. UJT RELAXATION OSCILLATOR

Aim: To obtain the characteristics of UJT Relaxation Oscillator.

Apparatus Required:

Name of the Component/Equipment	Specifications	Quantity
UJT	2N 2646	1
Resistors	220Ω	1
	68KΩ	1
	120Ω	1
Capacitor	0.1µF	1
	0.01µF	1
	0.001µF	1
Diode	0A79	1
Inductor	130mH	1
CRO	20MHz	1
Function generator	1MHz	1
Regulated Power Supply	(0-30V),1A	1

Circuit diagram:



Procedure:

1) Connect the circuit as shown in figA.

2) Observe the voltage waveform across the capacitor,C.

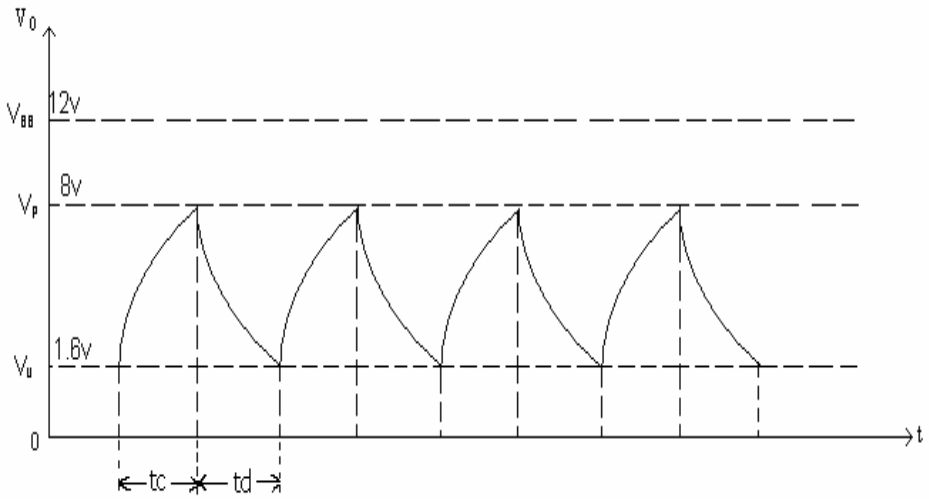
3) Change the time constant by changing the capacitor values to 0.1µF and 0.001 µF and observe the wave forms.

4) Note down the parameters, amplitude,charging and discharging periods of the wave forms

5)Compare the theoretical and practical time periods.

6)Plot the graph between voltage across capacitor with respect to time

Model graph:



13. BOOT STRAP SWEEP CIRCUIT

Aim: To observe the characteristics of a boot strap sweep circuit.

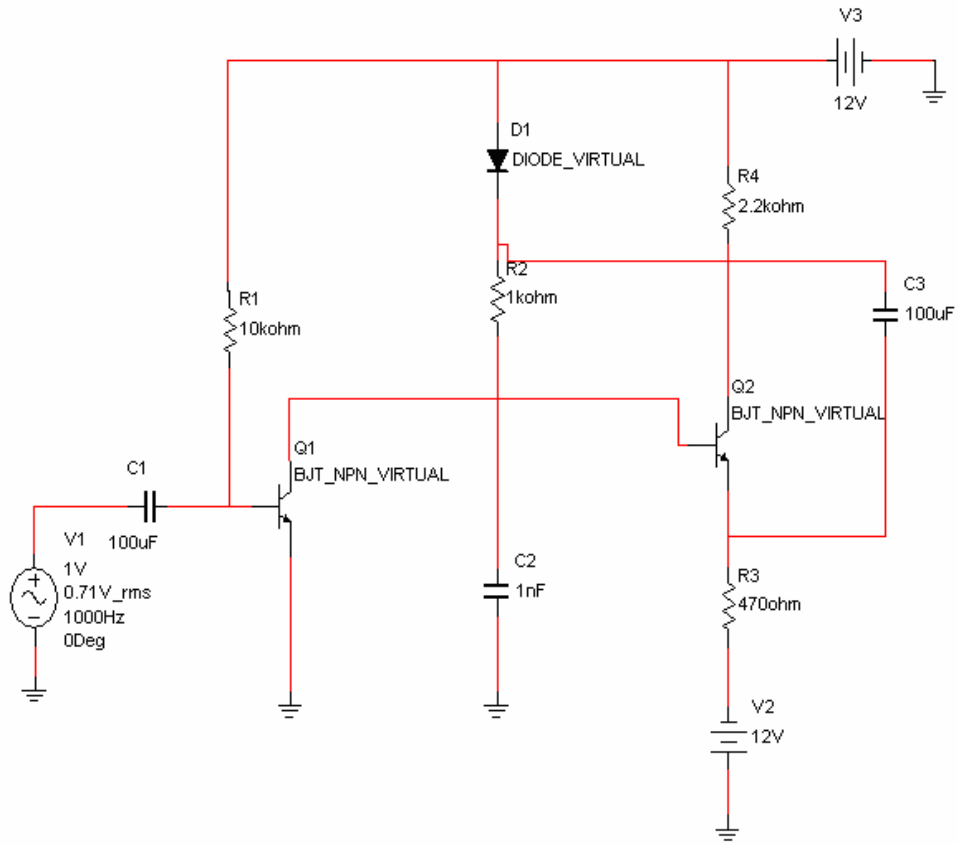
Apparatus Required:

Name of the Component/Equipment	Specifications	Quantity
Transistor	BC 107	2
Resistors	220Ω	1
	1KΩ	1
	470 Ω	1
	10Ω	1
Capacitor	100µF	2
	1µF	1
	0.001µF	1
Diode	2N2222	1
CRO	20MHz	1
Function generator	1MHz	1
Regulated Power Supply	(0-30V),1A	1

Theory:

Boot strap sweep generator is a technique used to generate a sweep with relatively less slope error when compared to the exponential sweep. This is achieved by maintaining a constant current through a resistor,by maintaing a constant voltage across it In the circuit shown Q1 acts as a switch which should be opened to initiate the sweep.Voltage across resistor is maintained constant (Vce) hence a constant current (Vcc/r) will charge the capacitor C.Transistor Q2 will act as an amplifier with high input impedance and voltage gain '1' (emitter follower) .Hence the same sweep which is generated across C will also appear at the output.

Circuit diagram:



Design equations:

$T_S(max)=RC$

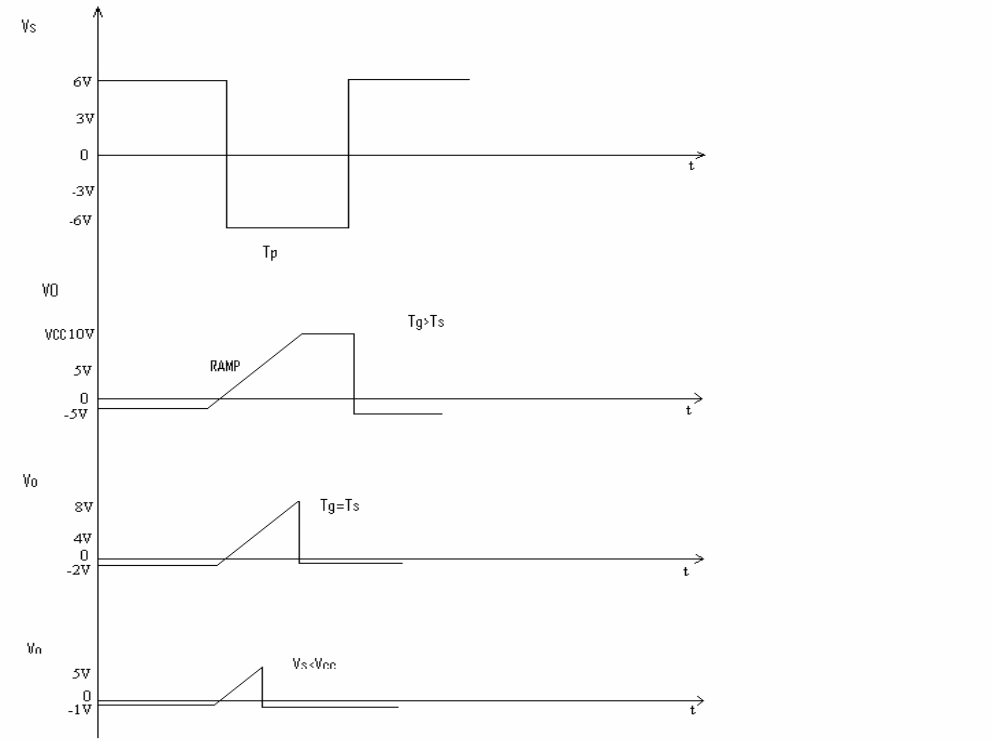
Assume 'C' and find 'R' for given maximum sweep

Select R_b to provide enough bias for switching transistor Q1

Procedure:

1. Connect the circuit as shown in the figure.
2. Apply the square wave input to the circuit (which is generated in the module itself).
3. Observe the output wave form.
4. By varying the input frequency observe the variations in the output.
5. Note the maximum value of sweep and starting voltage.
6. Note the sweep time Ts.

Wave forms:


Vs
6V
3V
0
-3V
-6V
t
Tp
VO
VCC 10V
5V
0
-5V
RAMP
Tg>Ts
t
Vo
8V
4V
0
-2V
Tg=Ts
t
Vo
5V
0
-1V
Vs<Vcc
t