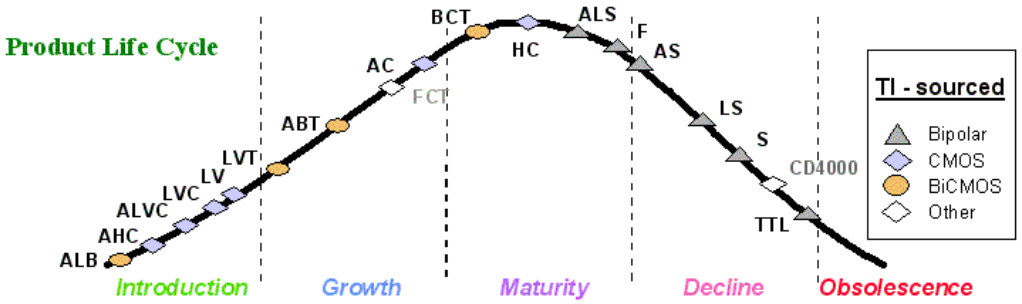


Digital Logic Families

A Laxman

Assistant Professor

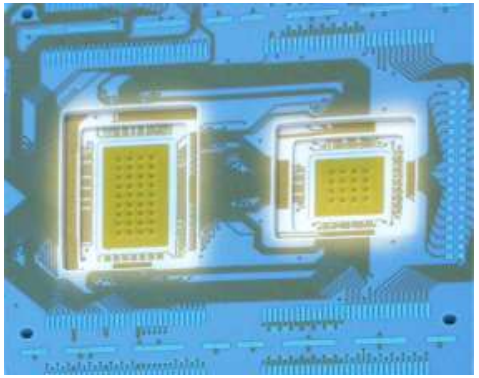
ECE Department

Overview

- Integration, Moore’s law
- Early families (DL, RTL)
- TTL
- Evolution of TTL family
- ECL
- CMOS family and its evolution
- Overview

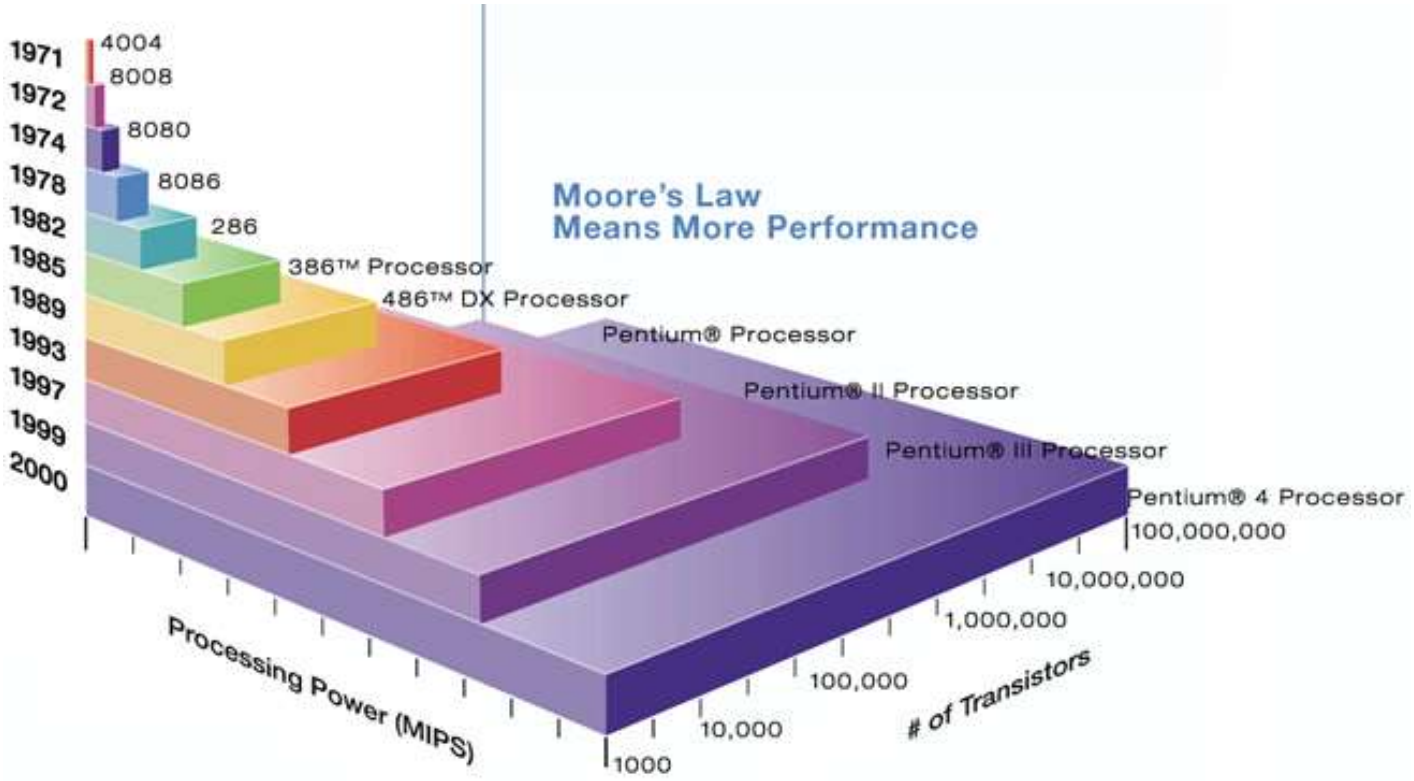
Integration Levels

- Gate/transistor ratio is roughly 1/10
  - SSI < 12 gates/chip
  - MSI < 100 gates/chip
  - LSI …1K gates/chip
  - VLSI …10K gates/chip
  - ULSI …100K gates/chip
  - GSI …1Meg gates/chip



Moore's law

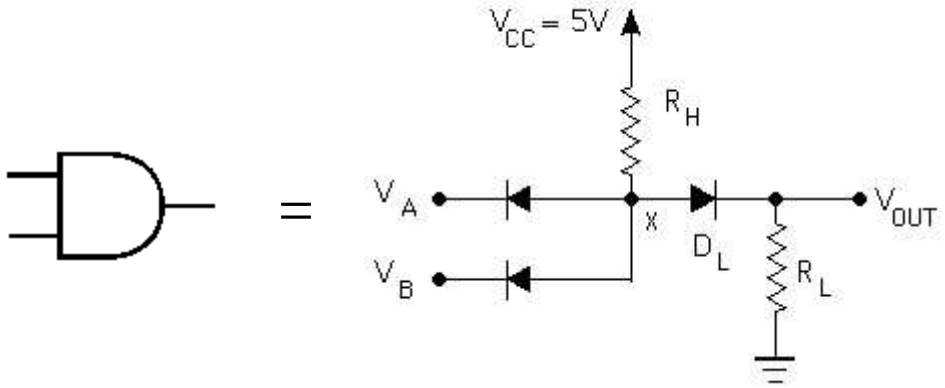
- A prediction made by Moore (a co-founder of Intel) in 1965: "… a number of transistors to double every 2 years."



In the beginning…

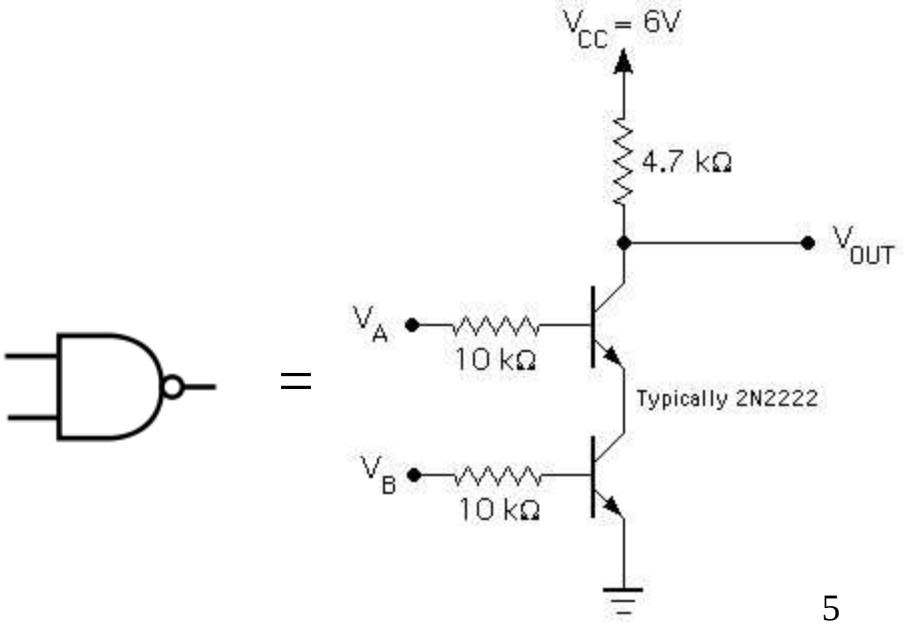
Diode Logic (DL)

- simplest; does not scale
- NOT not possible (need an active element)



Resistor-Transistor Logic (RTL)

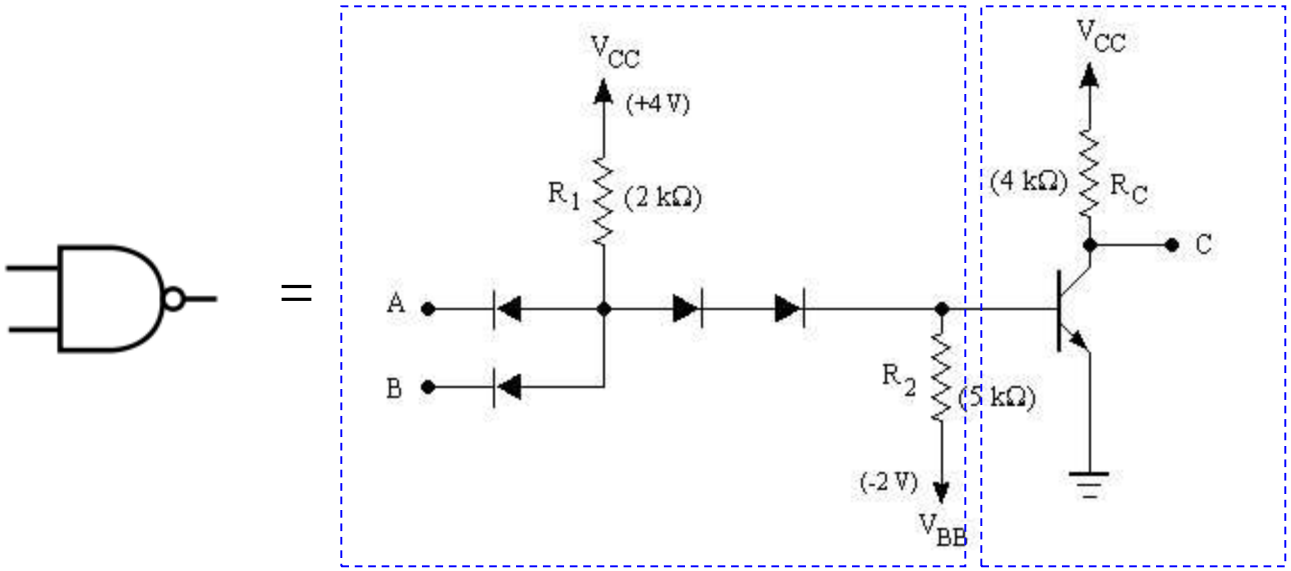
- replace diode switch with a transistor switch
- can be cascaded
- large power draw



was…

Diode-Transistor Logic (DTL)

- essentially diode logic with transistor amplification
- reduced power consumption
- faster than RTL



DL AND gate

Saturating inverter

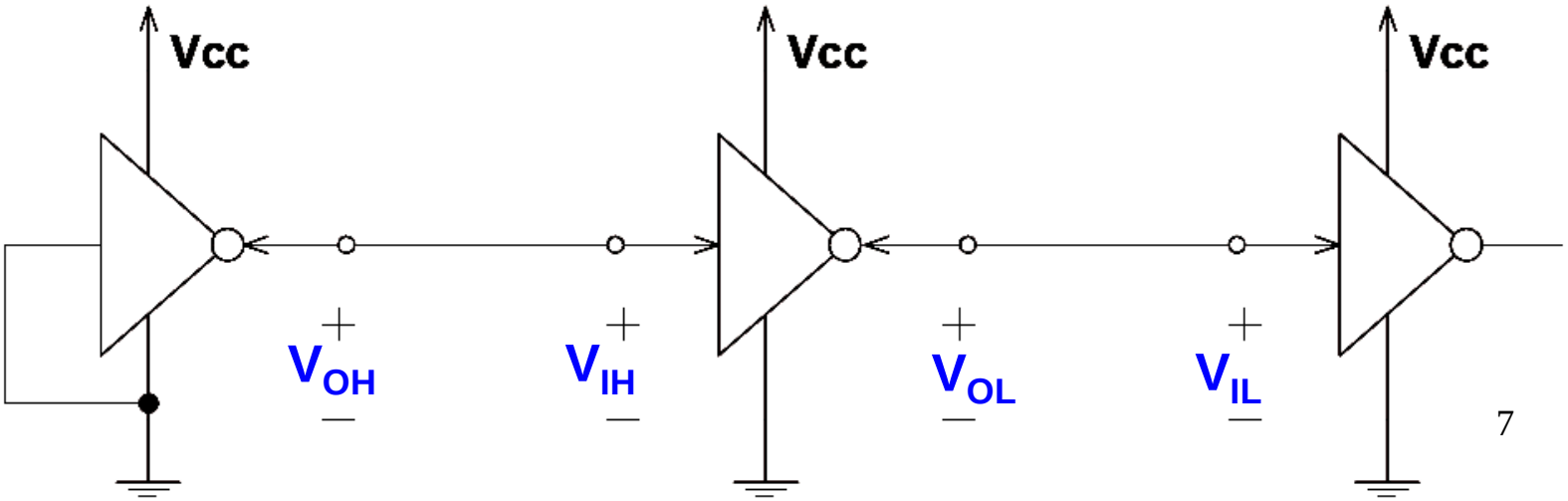
Logic families: V levels

V_{OH}(min) – The minimum voltage level at an output in the logical "1" state under defined load conditions

V_{OL}(max) – The maximum voltage level at an output in the logical "0" state under defined load conditions

V_{IH}(min) – The minimum voltage required at an input to be recognized as "1" logical state

V_{IL}(max) – The maximum voltage required at an input that still will be recognized as "0" logical state



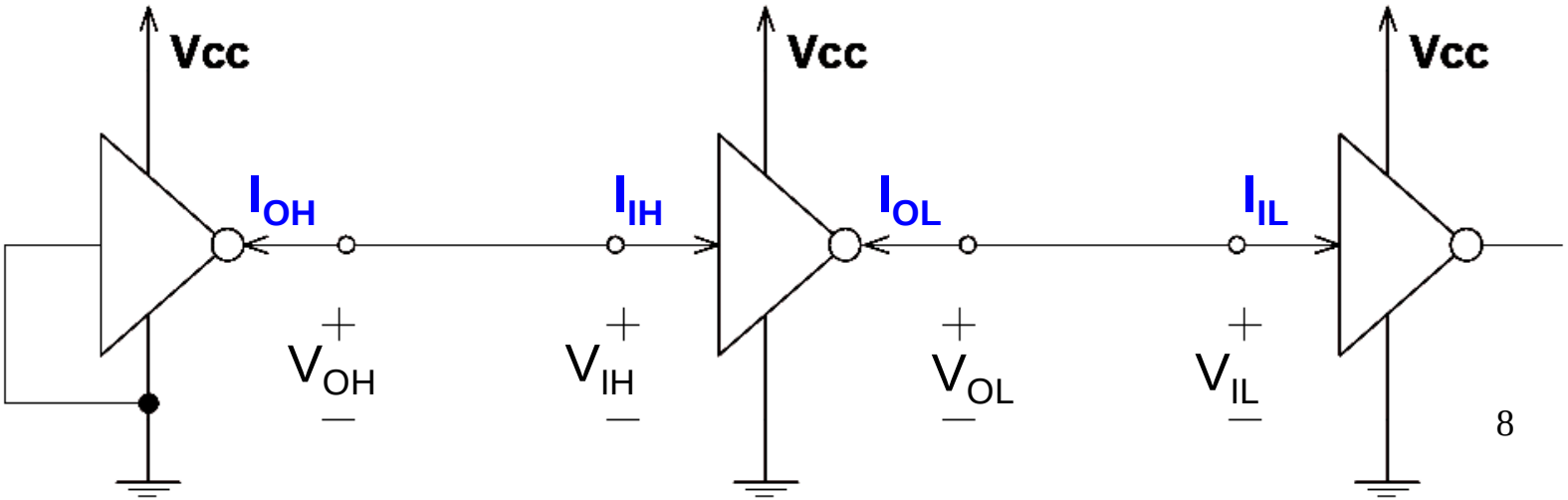
Logic families: I requirements

I_{OH} – Current flowing into an output in the logical "1" state under specified load conditions

I_{OL} – Current flowing into an output in the logical "0" state under specified load conditions

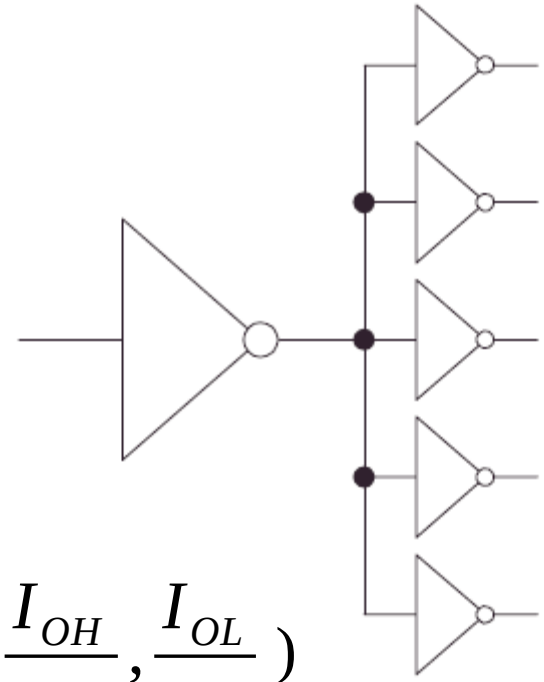
I_{IH} – Current flowing into an input when a specified HI level is applied to that input

I_{IL} – Current flowing into an input when a specified LO level is applied to that input



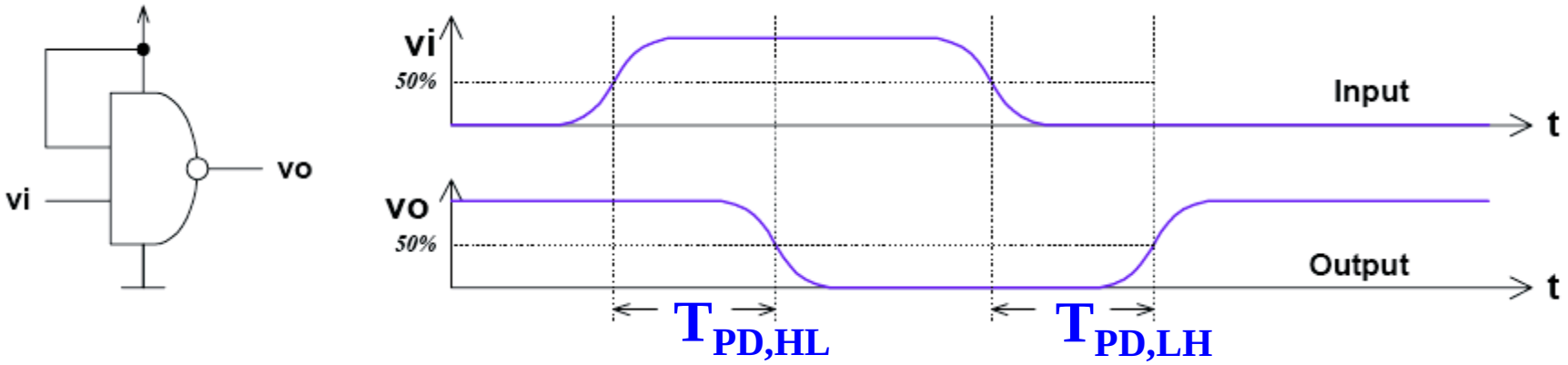
Logic families: fanout

Fanout: the maximum number of logic inputs (of the same logic family) that an output can drive reliably



DC fanout = $\min\left(\frac{I_{OH}}{I_{IH}}, \frac{I_{OL}}{I_{IL}}\right)$

Logic families: propagation delay

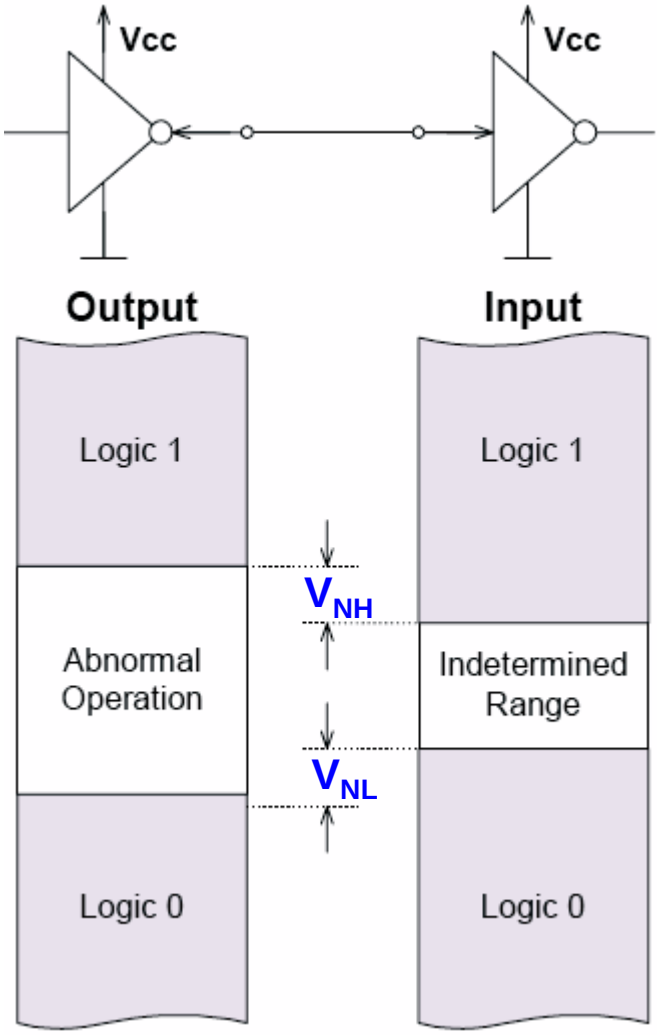


$T_{PD,HL}$ – input-to-output propagation delay from HI to LO output

$T_{PD,LH}$ – input-to-output propagation delay from LO to HI output

Speed-power product: $T_{PD} \times P_{avg}$

Logic families: noise margin



HI state noise margin:

$V_{NH} = V_{OH}(min) - V_{IH}(min)$

LO state noise margin:

$V_{NL} = V_{IL}(max) - V_{OL}(max)$

Noise margin:

$V_N = min(V_{NH}, V_{NL})$

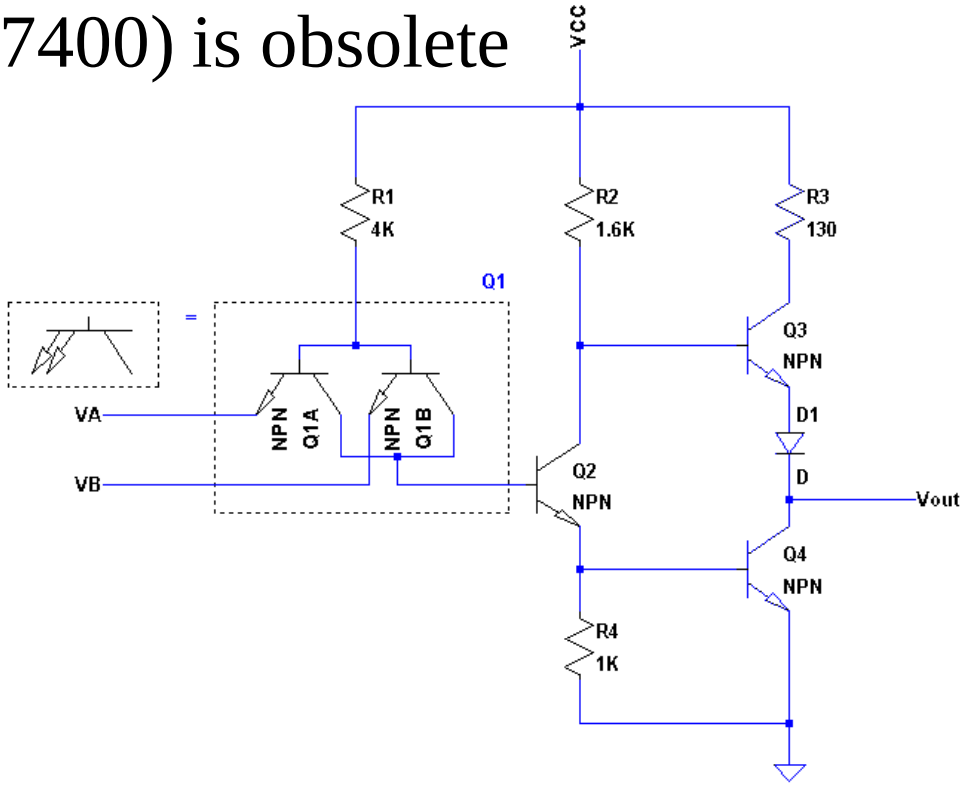
TTL

Bipolar Transistor-Transistor Logic (TTL)

- first introduced by in 1964 (Texas Instruments)
- TTL has shaped digital technology in many ways
- Standard TTL family (e.g. 7400) is obsolete
- Newer TTL families still used (e.g. 74ALS00)

Distinct features

- Multi-emitter transistors
- Totem-pole transistor arrangement
- Open LTspice example: TTL NAND…



2-input NAND

ECL

Emitter-Coupled Logic (ECL)

- PROS: Fastest logic family available (~1ns)
- CONS: low noise margin and high power dissipation
- Operated in emitter coupled geometry (recall differential amplifier or emitter-follower), transistors are biased and operate near their Q-point (never near saturation!)
- Logic levels. “0”: –1.7V. “1”: –0.8V
- Such strange logic levels require extra effort when interfacing to TTL/CMOS logic families.
- Open LTspice example: ECL inverter…

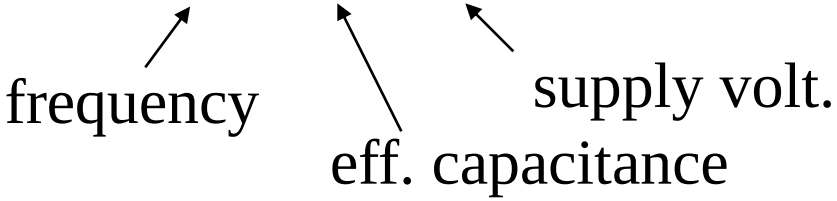
CMOS

Complimentary MOS (CMOS)

- Other variants: NMOS, PMOS (obsolete)
- Very low static power consumption
- Scaling capabilities (large integration all MOS)
- Full swing: rail-to-rail output
- Things to watch out for:
  - don't leave inputs floating (in TTL these will float to HI, in CMOS you get undefined behaviour)
  - susceptible to electrostatic damage (finger of death)
- Open LTspice example: CMOS NOT and NAND…

CMOS/TTL power requirements

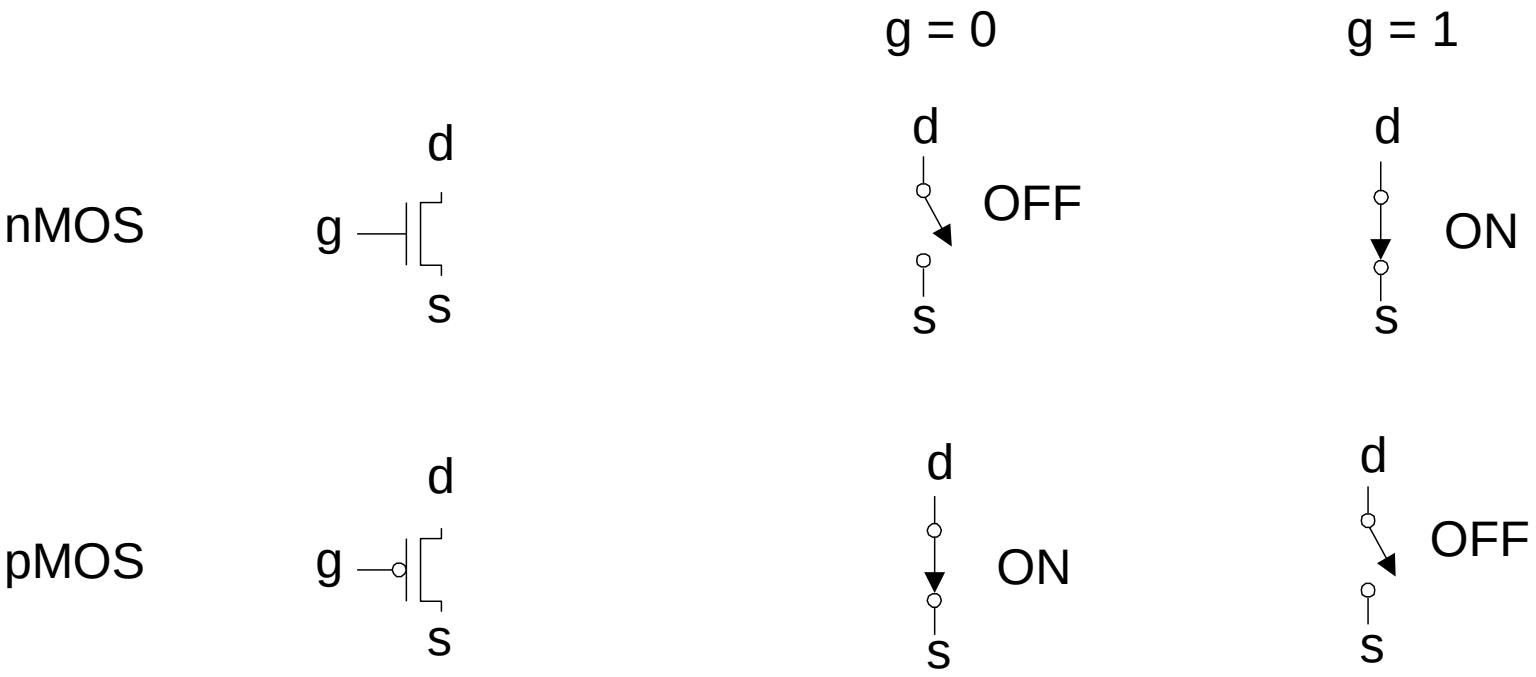
- TTL power essentially constant (no frequency dependence)
- CMOS power scales as $\propto f \times C \times V^2$



- At high frequencies (>> MHz) CMOS dissipates more power than TTL
- Overall advantage is still for CMOS even for very fast chips – only a relatively small portion of complicated circuitry operates at highest frequencies

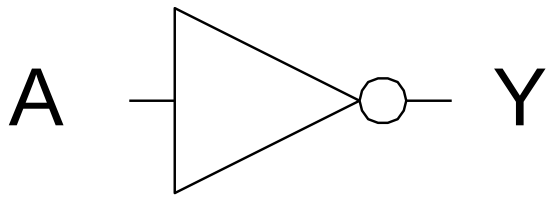
Transistors as Switches

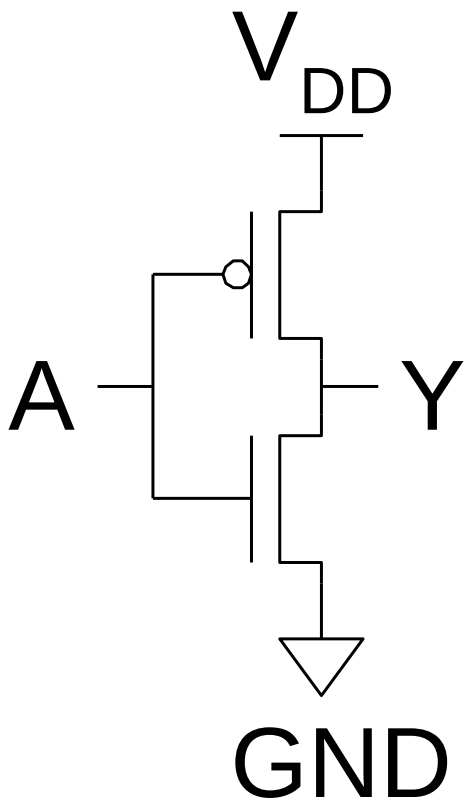
- We can view MOS transistors as electrically controlled switches
- Voltage at gate controls path from source to drain



CMOS Inverter

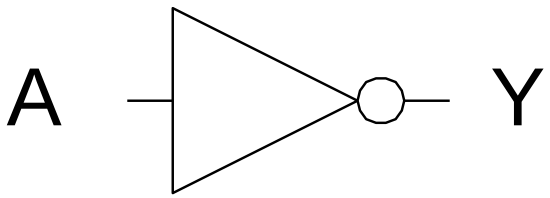
A	Y
0	
1	

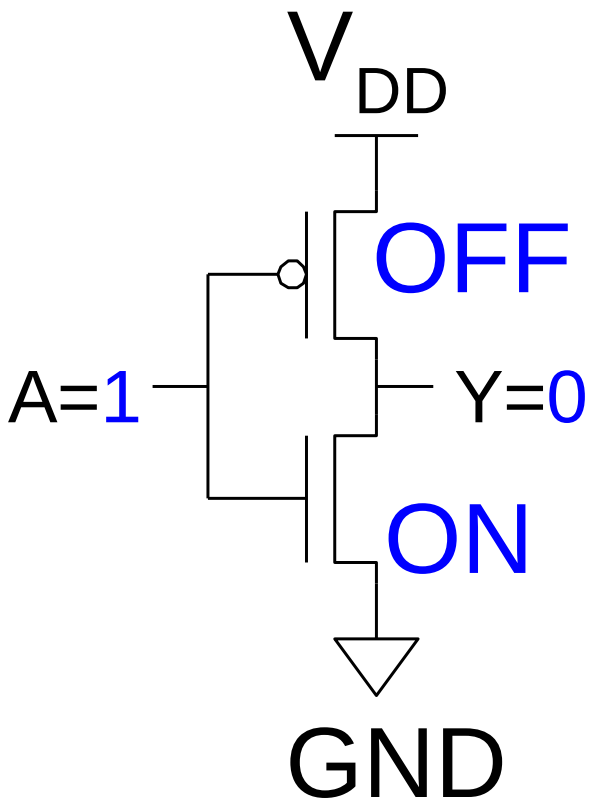




CMOS Inverter

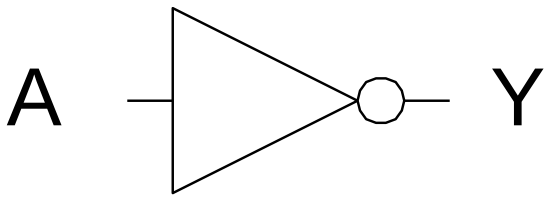
A	Y
0	
1	**0**

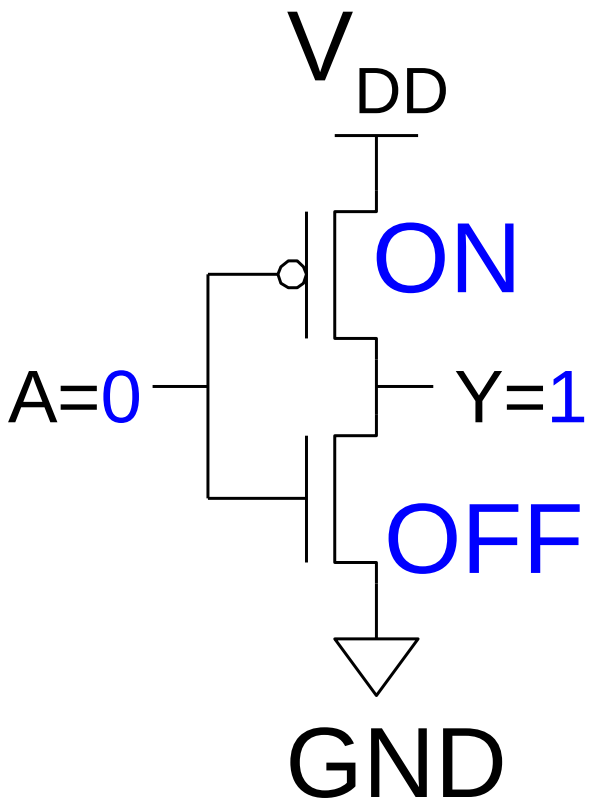




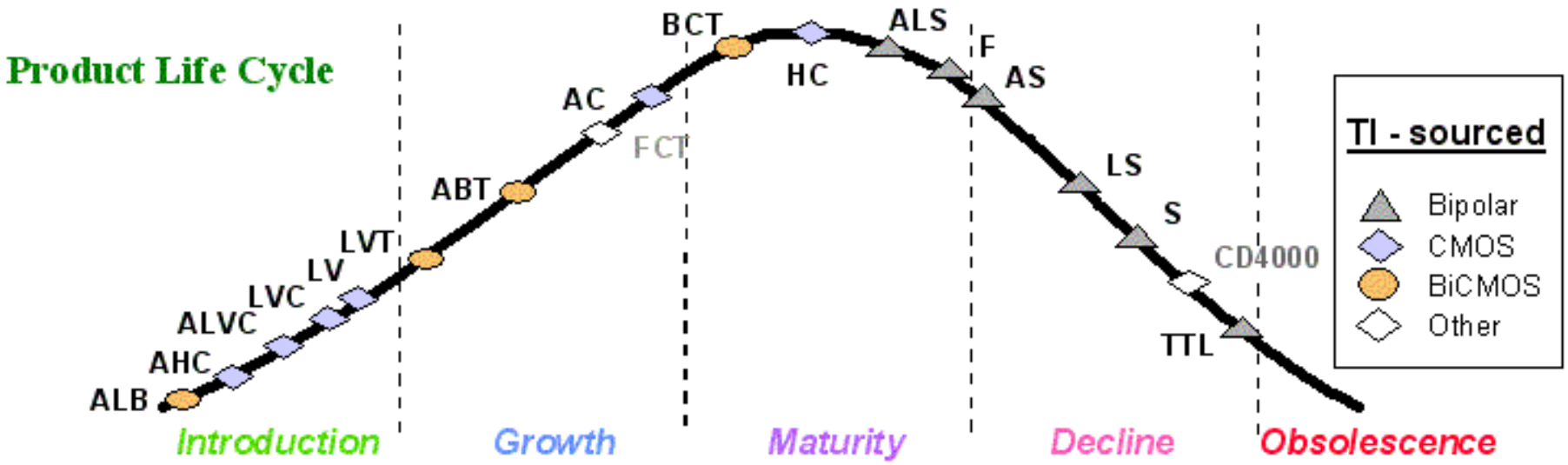
CMOS Inverter

A	Y
0	**1**
1	0





Life-cycle


Product Life Cycle
ALB
AHC
ALVC
LVC
LV
LVT
ABT
AC
FCT
BCT
HC
ALS
F
AS
LS
S
CD4000
TTL
Introduction
Growth
Maturity
Decline
Obsolescence
TI - sourced
Bipolar
CMOS
BiCMOS
Other

Thank you