Mahaveer Institute of Science & Technology

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(Approved by AICTE, Affiliated to JNTUH)

(A Constitute college of Mahaveer Educational society)

EAMCET CODE : MIST, JNTUH College code:E3

IC APPLICATIONS AND HDLSIMULATION
LABORATORY MANUAL

ECE III Year I SEMESTER

DEPARTMENT OF ELECTRONICS & COMMUNICATION
ENGINEERING
List of Experiments

CYCLE - 1

LINEAR IC LAB

1. OP AMP Applications – Adder, Subtractor, Comparator Circuits.
2. Integrator and Differentiator Circuits using IC 741.
3. Active Filter Applications – LPF, HPF (first order)
4. IC 741 WAVES FORM GENERATORS.
5.1. IC 555 Timer – Monostable Operation Circuit.
5.2. IC 555 Timer – Astable Operation Circuit.
7. IC 565 – PLL Applications.

8.1. Voltage Regulator using IC 723.
8.2. Three Terminal Voltage Regulators – 7805, 7809, 7912.

CYCLE – 2

1. HDL code to realize all logic gates.
2. Design of 2- to -4 decoder.
3. Design of 8 to 3 encoder
4. Design of 8 to 1 multiplexer and 1x8 demultiplexer.
5. Design of 4 bit binary to Gray code converter.
7. Design of Full adder using 3 modeling styles.
8. Design of flip-flops: SR,D,JK,T.
9. Design of 4-BIT binary , BCD counters.
10. Finite State Machine design.
1. OPAMP APPLICATIONS - ADDER, SUBTRACTOR, COMPARATOR CIRCUITS

AIM:
To study the applications of IC 741 as adder, subtractor, comparator

APPARATUS:
1. IC 741
2. Resistors (1KΩ) — 4
3. Function generator
4. Regulated power supply
5. IC bread board trainer
6. CRO
7. Patch cards and CRO probes

CIRCUIT

DIAGRAM: Adder:

Subtractor:
Comparator:

THEORY:

ADDER:

Op-Amp may be used to design a circuit whose output is the sum of several input signals such as circuit is called summing amplifier or summer. We can obtain either inverting or non-inverting summer.

The circuit diagrams shows a two input inverting summing amplifier. It has two input voltages $V_1$ and $V_2$, two input resistors $R_1$, $R_2$ and a feedback resistor $R_f$.

Assuming that op-amp is in ideal conditions and input bias current is assumed to be zero, there is no voltage drop across the resistor $R_{\text{Comp}}$ and hence the noninverting input terminal is at ground potential.

By taking nodal equations.

$$V_1/R_1 + V_2/R_2 + V_0/R_f = 0$$
$$V_0 = [(R_f/R_1) V_1 + (R_f/R_2) V_2]$$
And here $R_1 = R_2 = R_f = 1 \text{K} \Omega$
$$V_0 = -(V_1 + V_2)$$
Thus output is inverted and sum of input.
**SUBTRACTOR:**

A basic differential amplifier can be used as a subtractor. It has two input signals V1 and V2 and two input resistances R1 and R2 and a feedback resistor Rf. The input signals scaled to the desired values by selecting appropriate values for the external resistors.

From the figure, the output voltage of the differential amplifier with a gain of ‘1’ is

\[ V_0 = -\frac{R}{R_f} (V_2 - V_1) \]

\[ V_0 = V_1 - V_2. \]

Also \( R_1 = R_2 = R_f = 1 \, K\Omega. \)

Thus, the output voltage \( V_0 \) is equal to the voltage \( V_1 \) applied to the non inverting terminal minus voltage \( V_2 \) applied to inverting terminal. Hence the circuit is subtractor.

**COMPARATOR:**

A comparator is a circuit which compares a signal voltage applied to one input of an op-amp with a known reference voltage at the other input. It is basically an open loop op-amp with output ±Vs(\text{sat}) as in the ideal transfer characteristics.

It is clear that the change in the output state takes place with an increment in input \( Vi \) of only 2mv. This is the uncertainty region where output cannot be directly defined. There are basically 2 types of comparators.

1. Non inverting comparator and.
2. Inverting comparator.

The applications of comparator are zero crossing detector, window detector, time marker generator and phase meter.

**OBSERVATIONS: ADDER:**

<table>
<thead>
<tr>
<th>( V_1 ) (volts)</th>
<th>( V_2 ) (volts)</th>
<th>Theoretical ( V_0 = -(V_1 + V_2) )</th>
<th>Practical ( V_0 = -(V_1 + V_2) )</th>
</tr>
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SUBTRACTOR:

<table>
<thead>
<tr>
<th>$V_1$(volts)</th>
<th>$V_2$(volts)</th>
<th>Theoretical $V_0=(V_1-V_2)$</th>
<th>Practical $V_0=(V_1-V_2)$</th>
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</table>

COMPARATOR:

<table>
<thead>
<tr>
<th>Voltage input</th>
<th>$V_{ref}$</th>
<th>Observed square wave Amplitude</th>
</tr>
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MODEL GRAPH:

![Graph showing waveforms](image)

PROCEDURE:

ADDER:

1. Connections are made as per the circuit diagram.
2. Apply input voltage 1) $V_1=5v$, $V_2=2v$
   2) $V_1=5v$, $V_2=5v$
   3) $V_1=5v$, $V_2=7v$.
3. Using Millimeter measure the dc output voltage at the output terminal.
4. For different values of $V_1$ and $V_2$ measure the output voltage.
SUBTRACTOR:

1. Connections are made as per the circuit diagram.
2. Apply input voltage
   1) $V_1=5v, V_2=2v$
   2) $V_1=5v, V_2=5v$
   3) $V_1=5v, V_2=7v$.
3. Using multi meter measure the dc output voltage at the output terminal.
4. For different values of $V_1$ and $V_2$ measure the output voltage.

COMPARATOR:

1. Connections are made as per the circuit diagram.
2. Select the sine wave of 10V peak to peak, 1K Hz frequency.
3. Apply the reference voltage 2V and trace the input and output wave forms.
4. Superimpose input and output waveforms and measure sine wave amplitude with reference to $V_{ref}$.
5. Repeat steps 3 and 4 with reference voltages as 2V, 4V, -2V, -4V and observe the waveforms.
6. Replace sine wave input with 5V dc voltage and $V_{ref}=0V$.
7. Observe dc voltage at output using CRO.
8. Slowly increase $V_{ref}$ voltage and observe the change in saturation voltage.

PRECAUTIONS:

1. Make null adjustment before applying the input signal.
2. Maintain proper Vcc levels.

RESULT:
2. OP-AMP741 AS DIFFRENTIATOR AND INTEGRATOR

AIM:

To design and test an op-amp differentiator and integrator

EQUIPMENTS AND COMPONENTS:

APPARATUS

1. DC power supply - 1 No.
2. CRO - 1 No.
3. Bread Board - 1 No.
4. Function Generator - 1 No.

COMPONENTS:

1. 15 kΩ Resistor – 2 No.
2. 820 Resistor – 1 No.
3. 1.5 kΩ Resistor – 1 No.
4. 0.01 F Capacitor – 2 No
5. 0.5 nF Capacitor – 1 No
6. IC741 – 1 No.

THEORY

The operational amplifier can be used in many applications. It can be used as differentiator and integrator. In differentiator the circuit performs the mathematical operation of differentiation that is the output wave form is the derivative of the input waveform for good differentiation, one must ensure that the time period of the input signal is larger than or equal to RfC1. the practical differentiator eliminates the problem of instability and high frequency noise.

CIRCUITDIAGRAM:

![Circuit Diagram](image)
PROCEDURE:

1. Connect the differentiator circuit as shown in Fig 1. Adjust the signal generator to produce a 5 volt peak sine wave at 100 Hz.
2. Observe input $V_i$ and $V_o$ simultaneously on the oscilloscope measure and record the peak value of $V_o$ and the phase angle of $V_o$ with respect to $V_i$.
3. Repeat step 2 while increasing the frequency of the input signal. Find the maximum frequency at which circuit offers differentiation. Compare it with the calculated value of $f_d$. Observe & Sketch the input and output for square wave.
4. Connect the integrator circuit shown in Fig 2. Set the function generator to produce a square wave of 1V peak-to-peak amplitude at 500Hz. View simultaneously output $V_o$ and $V_i$.
5. Slowly adjust the input frequency until the output is good triangular waveform. Measure the amplitude and frequency of the input and output waveforms.
6. Verify the following relationship between $R_iC_i$ and input frequency for good integration $f_i > f_d$ and $T < R_iC_i$
   Where $R_iC_i$ is the time constant
7. Now set the function generator to a sine wave of 1V peak-to-peak and frequency 500Hz. Adjust the frequency of the input until the output is a negative going cosine wave. Measure the frequency and amplitude of the input and output waveforms.

OBSERVATIONS:

1. The time period and amplitude of the output waveform of differentiator circuit
2. The time period and amplitude of the integrator waveform

CALCULATIONS:

Design a differentiator to differentiate an input signal that varies in frequency from 10 Hz to 1 kHz.

$$f_d = \frac{1}{2R_iC_i}$$

$f_i = 1$ kHz, the highest frequency of the input signal
Let $C_i = 0.01$ F,
Then $R_i = 15.9$ k
Therefore choose $R_i = 15.0$ k

$$f_d = \frac{1}{2R_iC_i}$$

Choose: $f_i = 20x$ $f_d = 20$ KHz
Hence $R_i = 795$
Therefore choose $R_i = 820$
Since $R_iC_i = R_iC_i$ (compensated attenuator)
$C_i = 0.54$ nF
Therefore choose $C_i = 0.5$ nF

Integrator: Design an integrator that integrates a signal whose frequencies are between 1 KHz and 10 KHz
\[ f_b = \frac{1}{2R_1C_f} \]

The frequency at which the gain is 0 dB.

\[ f_a = \frac{1}{2R_fC_f} \]

\( f_a \): Gain limiting frequency.
The circuit acts as integrator for frequencies between \( f_a \) and \( f_b \).
Generally \( f_b < f_a \) [Ref. Frequency response of the integrator]

Therefore choose \( f_a = 1 \text{KHz} \)

Let \( C_f = 0.01 \text{ F} \)

Therefore \( R_1 = 1.59k \)

Choose \( R_1 = 1.5 \text{ K} \)

\( R_c = 15 \text{ K} \)

**GRAPH:**
**Differentiator**

![Graph](image-url)
Integrator

\[ v_i, v_0 \]

(a)

\[ v_1 \]

(b)

\[ v_i, v_0 \]

(c)
RESULT:
3. ACTIVE FILTER APPLICATIONS - LPF, HPF [ FIRSTORDER ]

AIM:
To study Op-Amp as first order LPF and first order HPF and to obtain frequency response.

APPARATUS:
1. IC 741.
2. Resistors (10KΩ--2, 560Ω, 330Ω)
3. Capacitors(0.1Ω)
4. Bread board trainer
5. CRO
6. Function generator
7. connecting wires
8. Patch cards.

CIRCUIT

DIAGRAM: (a)

LPF
(a) HPF

THEORY:

LOWPASS FILTER:

The first order low pass butter worth filter uses an Rc network for filtering. The op-amp is used in the noninverting configuration, hence it does not load down the RC network. Resistor R1 and R2 determine the gain of the filter.

\[ V_0/Vin = A_f/(1+jf/f_h) \]

\[ A_f = 1 + R_f/R_1 = \text{pass band gain of filter} \]

\( f = \text{frequency of the input signal.} \)

\( f_h = 1/2\pi RC = \text{High cut off frequency of filter} \)

\( V_0/Vin = \text{Gain of the filter as a function of frequency} \)

The gain magnitude and phase angle equations of the LPF the can be obtained by converting \( V_0/Vin \) into its equivalent polar form as follows

\[ |V_0/Vin| = A_f/\sqrt{1+(f/f_h)^2} \]

\[ \Phi = - \tan^{-1}(f/f_h) \]

Where \( \Phi \) is the phase angle in degrees. The operation of the LPF can be verified from the gain magnitude equation.
1. At very low frequencies i.e. \( f < f_h \),
\[ |V_0/V_{in}| = A_f. \]
2. At \( f = f_h \),
\[ |V_0/V_{in}| = A_f/\sqrt{2}. \]
3. At \( f > f_h \),
\[ |V_0/V_{in}| < A_f. \]

**HIGH PASS FILTER:**

High pass filters are often formed simply by interchanging frequency. Determining resistors and capacitors in LPFs that is, a first order HPF is formed from a first order LPF by interchanging components ‘R’ and ‘C’ figure. Shows a first order butter worth HpF with a lower cut off frequency of ‘F’l. This is the frequency at which magnitude of the gain is 0.707 times its pass band value. Obviously all frequencies, with the highest frequency determinate by the closed loop band width of op-amp.

For the first order HPF, the output voltage is

\[ V_0 = [1 + R_f/R_1] j2\Pi R C V_{in}/(1- j2\Pi fR C) \]

\[ V_0/V_{in} = A_f[j(f/f_l)]/(1- j(f/f_l))] \]

Where \( A_f + R_f/R_1 \) a pass band gain of the filter.

\( F\) = frequency of input signal.
\( F_l = 1/2\Pi R C = \) lower cut off frequency
Hence, the magnitude of the voltage gain is

\[ |V_0/V_{in}| = A_f(f/f_l)/\sqrt{1 + (f/f_l)^2}. \]

Since, HPFs are formed from LPFs simply by interchanging R’s and C’s. The design and frequency scaling procedures of the LPFs are also applicable to HPFs.

**PROCEDURE:**

1. Connections are made as per the circuit diagram.
2. Apply sine wave of amplitude 4Vp-p to the non inverting input terminal.
3. Values the input signal frequency.
4. Note down the corresponding output voltage.
5. Calculate gain in db.
6. Tabulate the values.
7. Plot a graph between frequency and gain.
8. Identify stop band and pass band from the graph.
OBSERVATIONS:

Low Pass Filter

<table>
<thead>
<tr>
<th>Frequency (Hz)</th>
<th>V₀ (V)</th>
<th>Gain in dB = $20 \log \left( \frac{V₀}{V_i} \right)$</th>
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MODEL GRAPH:

High Pass Filter

![Diagram of High Pass Filter](image)
PRECAUTIONS:

1. Make null adjustment before applying the input signal.
2. Maintain proper Vcc levels.

RESULT:
4. FUNCTION GENERATOR USING OP AMPS

AIM:
To generate triangular and square wave forms and to determine the time period of the waveforms.

APPARATUS:
1. Op-Amp IC 741 –2 Nos
2. Bread board IC trainer
3. Capacitor 0.1µF
4. Zener diodes (6.2V)—2 Nos
5. Resistors—10KΩ, 150KΩ, 1.5KΩ, 1MΩ, 8.2KΩ
6. Patch cards
7. Connecting wires

CIRCUIT DIAGRAM:
THEORY:

The function generator consists of a comparator U1 and an integrator A2. The comparator U2 compares the voltage at point P continuously with the inverting input i.e., at zero volts. When voltage at P goes slightly below or above zero volts, the output of U1 is at the negative or positive saturation level, respectively.

To illustrate the circuit operation let us set the output of U1 at positive saturation +Vs (approximately +Vcc). This +Vs is an input to the integrator U2. The output of U2, therefore will be a negative going ramp. Thus, one end of the voltage divider R2-R3 is the positive saturation voltage +V as to U1 and the other is the negative going ramp of U2. When the negative going ramp attains a certain value –Vramp, point P is slightly below zero volts; hence the output of U1 will switch from positive saturation to negative saturation –Vs (approximately –Vcc).

This means that the output of U2 will now stop going negatively and will begin to go positively. The output of U2 will continue to increase until it reaches +Vramp. At this time the point P is slightly above zero volts. The sequence then repeats. The frequencies of the square area function of the d.c supply voltage. Desired amplitude can be obtained by using approximate zener sat the output of U1.

THEORETICAL VALUES:

Time period, T=4R5C (R3+R4)/(R1+R2) =0.492 msec. 
Positive peak ramp =VzR5/(R1+R2) =0.05 volts.

PRACTICAL VALUES:

Time periods of triangular wave=
Time periods of square wave=
Positive peak ramp=
Voltage of square wave=

PROCEDURE:

1. The circuit is connected as shown in the figure.
2. The output of the comparator U1 is connected to the CRO through channel1, to generate a square wave.
3. The output of the comparator U2 is connected to the CRO through channel2, to generate a triangular wave.
4. The time periods of the square wave and triangular waves are noted and they are found to be equal.
MODEL GRAPH:

PRECAUTIONS:

1. Make null adjustment before applying the input signal.
2. Maintain proper Vcc levels.

RESULT:
5.1. IC 555 TIMER-MONOSTABLECIRCUIT

AIM:
To construct and study the operation of a mono stable multi vibrato using 555 IC timer.

APPARATUS:

1. 555 IC timer
2. Capacitors (0.1µF,0.01µF)
3. Resistors 10KΩ
4. Bread board IC trainer
5. CRO
6. Connecting wires and Patchcards

THEORY:

Mono stable multivibrator is also known as triangular wave generator. It has one stable and one quasi stable state. The circuit is useful for generating single output pulse of time duration in response to a triggering signal. The width of the output pulse depends only on external components connected to the op-amp. The diode gives a negative triggering pulse. When the output is +Vs, a diode clamps the capacitor voltage to 0.7V. Then, a negative going triggering impulse magnitude Vi passing through RC and the negative triggering pulse is applied to the positive terminal.

Let us assume that the circuit is in stable state. The output V0 is +Vs. The diode D1 conducts and Vc the voltage across the capacitor ‘C’ gets clamped to 0.7V. The voltage at the positive input terminal through R1, R2 potentiometer divider is +βVs. Now, if a negative trigger of magnitude Vi is applied to the positive terminal so that the effective signal is less than 0.7V, the output of the Op-Amp will switch from +Vs to –Vs. The diode will now get reverse biased and the capacitor starts charging exponentially to –Vs. When the capacitor charge Vc becomes slightly more negative than –βVs, the output of the op-amp switches back to +Vs. The capacitor ‘C’ now starts charging to +Vs through R until Vc is 0.7V.

\[
V_0 = V_f + (V_i - V_f) e^{-\frac{t}{RC}}
\]

\[
\beta = \frac{R_2}{R_1 + R_2}
\]

If Vsat >> Vp and R1 = R2 and β = 0.5,

Then, T = 0.69RC.
CIRCUIT DIAGRAM:

PROCEDURE:

1. Connections are made as per the circuit diagram.
2. Negative triggering is applied at the terminal 2.
3. The output voltage is measured by connecting the channel-1 at pin3.
4. The output voltage across capacitor is measured by connecting the channel-2 at the point ‘P’.
5. Theoretically the time period is calculated by $T=1.1R_1C_1$ where $R_1 = 10\,\text{K}\Omega$ and $C_1 = 0.1\,\text{µF}$.
6. Practically the charging and discharging timers are measured and theoretical value of time period is measured with practical value.
MODELGRAF:

PRECAUTIONS:

1. Make the null adjustment before applying the input signal.
2. Maintain proper Vcc levels.

RESULT:
5.2. IC 555 TIMER-ASTABLECIRCUIT

AIM:
To construct and study the operation of Astable multivibrator using 555 timer

APPARATUS:

1. IC 555 Timer
2. Resistors (10 KΩ, 4.7 KΩ)
3. Diode (IN 4007)
4. Capacitors (0.1µF, 0.01µF)
5. CRO
6. Patch cards
7. CRO Probes
8. Connecting wires

CIRCUIT DIAGRAM:
THEORY:

A simple OPAMP astable multivibrator is also called square wave generator and free running oscillator. The principle for the generation of square wave output is to force an OP_AMP to operate in the saturation region $\beta = \frac{R_2}{R_1+R_2}$ of the output is feedback to input. The output is also feedback to the negative input terminal after integrating by means of a RCLPF whenever the negative input just exceeds $V_{ref}$, switching takes place resulting in a square wave output. In anastable multivibrator, both states are quasi stable states.

$$V_c(t) = V_f + (V_i - V_f) e^{-t/RC}$$

$$V_c(t) = V_{sat} - V_{sat}(1+\beta)e^{-t/RC}$$

We get $T_1 = RC \ln \left( \frac{1+\beta}{1-\beta} \right)$

$$T = 2T_1 = 2RC \ln \left( \frac{1+\beta}{1-\beta} \right), \quad V_o(p-p) = 2V_{sat}$$

PROCEDURE:

1. Connections are made as per the circuit diagram.
2. Pins 4 and 8 are shorted and connected to power supply $V_{cc}(+5V)$
3. Between pins 8 and 7 resistor $R_1$ of 10KΩ is connected and between
   7 and 6 resistor $R_2$ of 4.7KΩ is connected. Pins 2 and 6 short circuited.
4. In between pins 1 and 5 a Capacitor of 0.01μF is connected.
5. The output is connected across the pin 3 and GND.
6. In between pins 6 and GND a Capacitor of 0.1μF is connected.
7. Theoretically without diode charging time $T_{cis}$ given by
   $$T_c = 0.69(R_1+R_2)C_1,$$
   Discharging time $T_{dis}$ given by $T_d = 0.69R_2C_1$
   The frequency $f$ is given by $f = 1.45/(R_1+2R_2)C_1$
   % of Duty cycle is $(T_c/(T_c+T_d))*100$
8. Practically $T_d$ and $T_c$ are measured and wave forms are noted and theoretical
   Values are verified with practical values
9. Connect diode between pins 7 and 2.
10. Theoretically with diode connected charging time is given by $T_c = 0.69R_1C_1$
    Discharging time is given by $T_d = 0.69R_2C_1$
11. Practically $T_d$ and $T_c$ are noted and verified with theoretical values
OBSERVATIONS:

<table>
<thead>
<tr>
<th></th>
<th>With diode</th>
<th>without diode</th>
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<tbody>
<tr>
<td>Theoretical</td>
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<tr>
<td>Practical</td>
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<td>Theoretical</td>
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<tr>
<td>Practical</td>
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</table>

MODEL GRAPH:

PRECAUTIONS:

1. Make null adjustment before applying the input signal.
2. Maintain proper Vcc levels.

RESULT:
6. SCHMIT TRIGGER USING IC 741

**Aim:**
To construct the Schmitt trigger using Ic 741

**Apparatus:**
1. 741 IC
2. Function Generator
3. Bread board
4. Resistors
5. Power supply
6. Connection wire

**Circuit Diagram**

![Circuit Diagram](image)

**PROCEDURE:**
1. Connect the ckt as shown in the fig.
2. Apply the i/p sine wave at pin no. 2 of IC 741
3. Observed the square wave o/p at pin 6 of IC 741
4. Measure UTP and LTP and compare them with theoretical values.

**RESULT:**

**PRECAUTIONS:**
1. Loose connections should be avoided
2. Switch ON the supply after verification of the ckt.
3. Wave forms and readings must be taken without parallax error.

**Questions:**
1. Schmitt trigger is basically?
2. Eccless Jordan arrangement is not necessary in a Schmitt trigger (yes/no)?
3. What is the o/p waveform of a schmitt trigger ckt?
4. Special type of bistable multivibrator is?
5. Define UTP.
7. IC 565 PLL

AIM:
1. To study the operation of NE565 PLL
2. To use NE565 as an multiplier

EQUIPMENTS AND COMPONENTS:

APPARATUS
1. DC power supply - 1 No.
2. CRO - 1 No.
3. BreadBoard - 1 No.
4. Function Generator - 1 No.

COMPONENTS:
1. 6.8 kΩ Resistor – 1 No.
2. 0.1 F Capacitor – 1 No.
3. 0.001 F Capacitor – 2 Nos
4. IC565 - 1 No.

THEORY:
The 565 is available as a 14-pin DIP package. It is produced by Signatone Corporation.
The output frequency of the VCO can be rewritten as
\[ f_o = \frac{0.25}{R_T C_T} \text{ Hz} \]
Where \( R_T \) and \( C_T \) are the external resistor and capacitor connected to pin8 and pin9. A value between 2k and 20k is recommended for \( R_T \). The VCO free running frequency is adjusted with \( R_T \) and \( C_T \) to be at the centre for the input frequency range.
PROCEDURE:

i. Connect the circuit using the component values as shown in the figure.

ii. Measure the free-running frequency of VCO at pin 4 with the input signal $V_{\text{in}}$ set to zero. Compare it with the calculated value $0.25/R_T C_T$.

iii. Now apply the input signal of 1Vpp square wave at 1kHz to pin 2.

iv. Connect 1 channel of the scope to pin 2 and display this signal on the scope.
V. Gradually increase the input frequency till the PLL is locked to the input frequency. This frequency $f_1$ gives the lower end of the capture range. Go on increasing the input frequency, till PLL tracks the input signal, say to a frequency $f_2$. This frequency $f_2$ gives the upper end of the lock range. If the input frequency is increased further the loop will get unlocked.

vi. Now gradually decrease the input frequency till the PLL is again locked. This is the frequency $f_3$, the upper end of the capture range. Keep on decreasing the input frequency until the loop is unlocked. This frequency $f_4$ gives the lower end of the lock range.

vii. The lock range $f_L = (f_2 - f_4)$ compare it with the calculated value of $\frac{7.8f_0}{12}$

Also the capture range is $f_c = (f_1 - f_4)$. Compare it with the calculated value of capture range.

$$f_c = \left(\frac{f_L}{(2)(3.6)(10^3)xC}\right)^{1/2}$$

viii. To use PLL as a multiplier, make connections as shown in fig. The circuit uses a 4-bit binary counter 7490 used as divide-by-5 circuit.

ix. Set the input signal at 1 Vpp square wave at 500 Hz.

x. Vary the VCO frequency by adjusting the 20K potentiometer till the PLL is locked. Measure the output frequency.

xi. Repeat step 9 and 10 for input frequency of 1 kHz and 1.5 kHz.

**OBSERVATIONS:**

- $f_0 = \underline{……}$
- $f_1 = \underline{……}$
- $f_2 = \underline{……}$
- $f_3 = \underline{……}$
- $f_4 = \underline{……}$

**CALCULATIONS:**

$$f_L = (f_2 - f_4) = \frac{7.8f_0}{12}$$

$$f_c = (f_1 - f_4) = \frac{f_L}{(2)(3.6)(10^3)xC)^{1/2}$$
RESULT:

fo = __________

fi = __________

fc = __________
8.1. VOLTAGE REGULATOR USING IC 723

AIM:
To plot the regulation characteristics of the given IC LM 723.

APPARATUS:
1. Bread board
2. IC LM 723
3. Resistors (7.8KΩ, 3.9KΩ)
4. RPS
5. DRB
6. Capacitors 100µF
7. Patch cards
8. Connecting wires

CIRCUIT DIAGRAM:
PROCEDURE:

(1).LINE REGULATION

1. Connections are made as per the circuit diagram
2. Power supply is connected to 12 and 7 terminals
3. Volt meter is connected to 10 and 7 terminals
4. By increasing the input voltage corresponding volt meter reading is noted.

(2). LOAD REGULATION

1. Connect the load to the terminals 10 and GND.
2. Keep the input voltage constant at which line regulation is obtained
3. The maximum load value is calculated from IC ratings.
4. Now, we decrease the load resistance and notedown the corresponding value
   Of the output in volt meter.
5. Plot the graph for load verses load regulation.

OBSERVATIONS:

(1). LINE REGULATION:

\[ V_{nl} = \]

<table>
<thead>
<tr>
<th>Line voltage (V)</th>
<th>Output voltage (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>
(2). LOAD REGULATION:

<table>
<thead>
<tr>
<th>Regulated output(V)</th>
<th>Load current(mA)</th>
<th>Load resistance(KΩ)</th>
<th>Load regulation</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

% REGULATION = \[\frac{(V_{nl} - V_{fl})}{V_{fl}}\] * 100

MODEL GRAPH:

PRECAUTIONS:

1. While taking their adding so regulated output voltage load regulation, keep the input voltage constant at 15V.
2. Do not increase the input voltage more than 30 V while taking their adding form load condition?

RESULT:
8.2. Three Terminal Voltage Regulators (7805, 7809 And 7912)

**AIM:**
To verify the operation of three terminal fixed voltage regulators 7805, 7809, 7912 and also to find out their line and load regulation.

**APPARATUS:**

<table>
<thead>
<tr>
<th>S.No.</th>
<th>Name of the component</th>
<th>Range</th>
<th>Quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>7805</td>
<td>--</td>
<td>1</td>
</tr>
<tr>
<td>2.</td>
<td>7809</td>
<td>--</td>
<td>1</td>
</tr>
<tr>
<td>3.</td>
<td>7912</td>
<td>--</td>
<td>1</td>
</tr>
<tr>
<td>4.</td>
<td>Capacitors</td>
<td>0.33µf</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.1µf</td>
<td>1</td>
</tr>
<tr>
<td>5.</td>
<td>Multimeter</td>
<td>(0-30)v</td>
<td>1</td>
</tr>
<tr>
<td>6.</td>
<td>Power Supply</td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>

**CIRCUIT DIAGRAM:**

![Circuit Diagram](image)
THEORY:
Three terminal voltage regulators have three terminals which are unregulated input ($V_{in}$), regulated output ($V_o$) and common or a ground terminal. These regulators do not require any feedback connections.

Positive voltage regulators:
78xx is the series of three terminal positive voltage regulators in which xx indicate the output voltage rating of the IC.

7805:
This is a three terminal regulator which gives a regulated output of $+5V$ fixed. The maximum unregulated input voltage which can be applied to 7805 is $35V$.

7809:
This is also three terminal fixed regulator which gives regulated voltage of $+9V$. Negative voltage regulators:
79xx is the series of negative voltage regulators which gives a fixed negative voltage as output according to the value of xx.

7912:
This is a negative three terminal voltage regulator which gives a output of $-12V$.

Line Regulation:
It is defined as the change in the output voltage for a given change in the input voltage. It is expressed as a percentage of output voltage or in millivolts.

$$\%R_{L} = \frac{\Delta V_o}{\Delta V_{in}} \times 100$$

Load Regulation:
It is the change in output voltage over a given range of load currents that is from full load to no load. It is usually expressed in millivolts or as a percentage of output voltage.

$$\%R_{Load} = \frac{(V_{nl}-V_{fl})}{V_{nl}} \times 100$$

PROCEDURE:
1. Connect the circuit as shown in the figure.
2. Apply unregulated voltage from $7.5V$ to $35V$ and observe the output voltage.
3. Calculate the line and load regulation for the regulator.
4. Plot the graphs from the observations.
5. Repeat the same for the remaining regulators.

Result